EM74LVC06A

Hex inverter with open-drain outputs

Product datasheet, Rev. 1.0 Oct 30, 2023

1.General Description

The 74LVC06A provides six inverting buffers. The outputs are open-drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2.Features and Benefits

■ Wide supply voltage range from 1.2 V to 5.5 V

■ Overvoltage tolerant inputs to 5.5 V

■ CMOS low power dissipation

■ I_{OFF} circuitry provides partial Power-down mode operation

■ Latch-up performance exceeds 250 mA

■ Direct interface with TTL levels

■ Complies with JEDEC standard:

- JESD8-7 (1.65 V to 1.95 V)
- JESD8-5 (2.3 V to 2.7 V)
- JESD8C (2.7 V to 3.6 V)
- JESD36 (4.5 V to 5.5 V)

■ ESD protection:

- HBM ANSI/ESDA/JEDEC JS-001 Class 3A exceeds 6000 V
- CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V

■ Multiple package options

3.Ordering Information

Table 1. Ordering information

Type number	Package		
	Name	Description	Quantity
EM74LVC06AD	SOP-14L	plastic small outline package; 14 leads; body width 3.9 mm	3000
EM74LVC06APW	TSSOP-14L	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	3000

4.Function Diagram

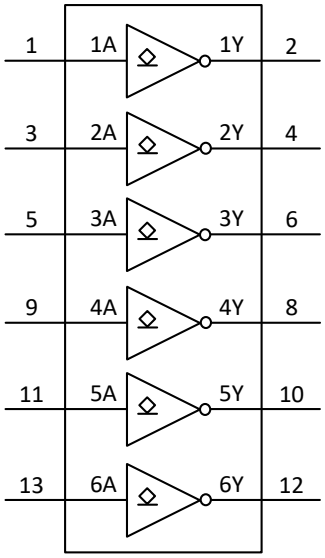

Fig. 1. Logic symbol

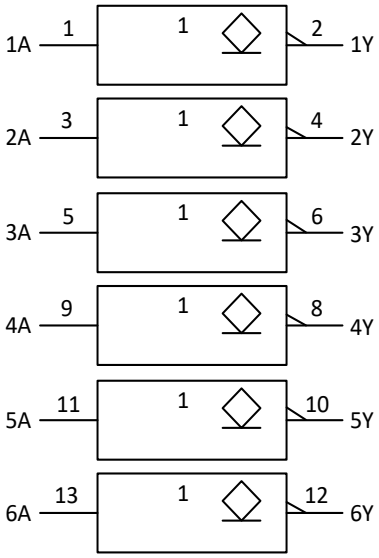

Fig. 2. IEC logic symbol

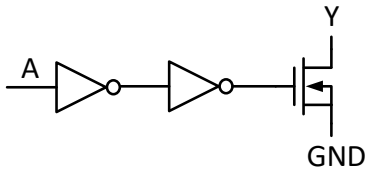

Fig. 3. Logic diagram (one gate)

5.Pinning Information

5.1. Pinning

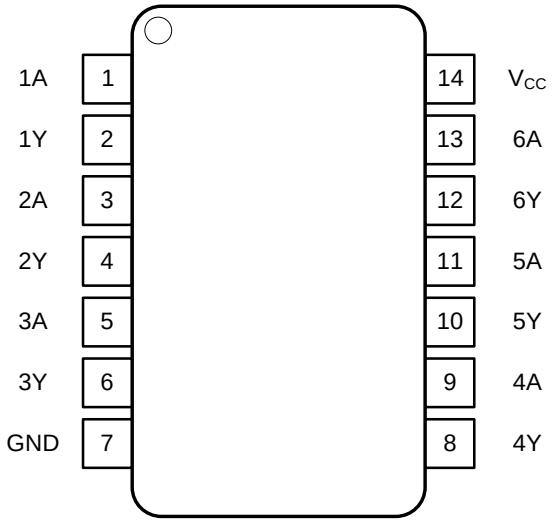

Fig. 4. Top view pin configuration SOP and TSSOP

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	Data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	Data output
GND	7	Ground (0V)
V_{CC}	14	Supply voltage

6.Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input nA	Output nY
L	Z
H	L