

## 1. General Description

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The EM74LVC02A is a quad 2-input NOR gate. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

## 2. Features and Benefits

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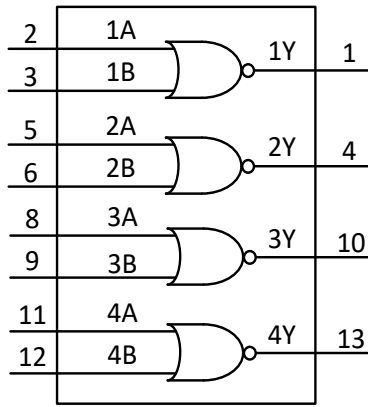
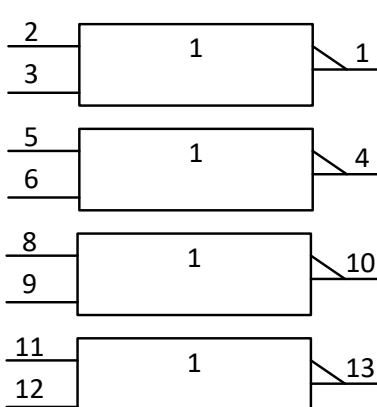
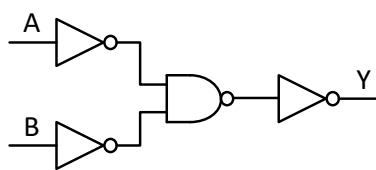
- Wide supply voltage range from 1.2 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- CMOS low power dissipation
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
  - JESD36 (4.5 V to 5.5 V)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 3A exceeds 6000 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options

### 3. Ordering Information

Table 1. Ordering information

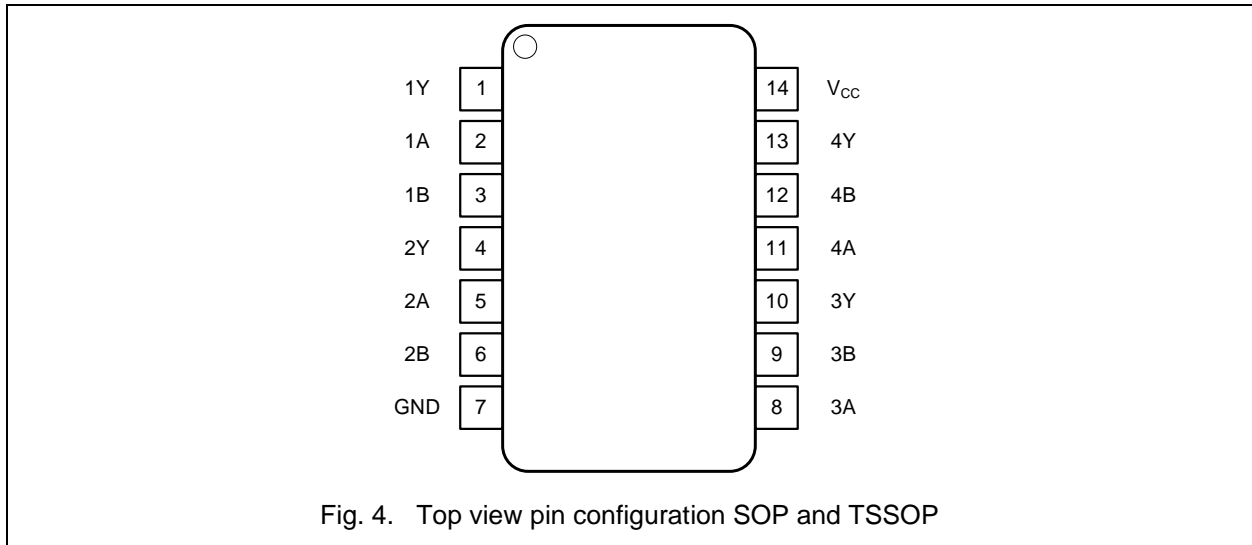
Type number	Package		
	Name	Description	Quantity
EM74LVC02AD	SOP-14L	plastic small outline package; 14 leads; body width 3.9 mm	3000
EM74LVC02APW	TSSOP-14L	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	3000

### 4. Function Diagram

 <p>Fig. 1. Logic symbol</p>	 <p>Fig. 2. IEC logic symbol</p>	 <p>Fig. 3. Logic diagram (one gate)</p>
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## 5. Pinning Information

### 5.1. Pinning



### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1Y, 2Y, 3Y, 4Y	1, 4, 10, 13	Data output
1A, 2A, 3A, 4A	2, 5, 8, 11	Data input
1B, 2B, 3B, 4B	3, 6, 9, 12	Data input
GND	7	Ground (0V)
V <sub>cc</sub>	14	Supply voltage

## 6. Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input nA	Input nB	Output nY
L	L	H
X	H	L
H	X	L