EM74LVC1G132

Single 2-input NAND gate with Schmitt trigger inputs

Product datasheet, Rev1.0 Oct 30, 2023

1.General Description

The EM74LVC1G132 is a single 2-input NAND gate with Schmitt-trigger inputs. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments. This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2.Features and Benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power dissipation
- I_{OFF} circuitry provides partial Power-down mode operation
- ±24 mA output drive (V_{CC} = 3.0 V)
- Latch-up performance exceeds 100 mA
- Direct interface with TTL levels
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
  - JESD36 (4.5 V to 5.5 V)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 3B exceeds 8000 V
  - MM JESD22-A115C Class C exceeds 550 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options

3.Ordering Information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Quantity
EM74LVC1G132GV	V∀YW	SOT23-5L	SOT23 package, 5 pins 2.92 mm × 1.6 mm; 1.25 mm (Max) height	3000
EM74LVC1G132GW	V∀YW	SOT353	SOT353 package, 5 pins 2.1 mm × 1.25 mm; 1.1 mm (Max) height	3000
EM74LVC1G132GS	V∀	DFN1x1-6L	DFN1×1 package, 6 pins 1 mm × 1 mm; 0.42 mm (Max) height	3000
EM74LVC1G132GM	V∀YW	DFN1x1.45-6L	DFN1.45×1 package, 6 pins 1.45 mm × 1 mm; 0.6 mm (Max) height	3000
EM74LVC1G132GX	V∀	DFN0.8x0.8-4L	DFN0.8×0.8 package, 5pins 0.8 mm × 0.8 mm; 0.4 mm (Max) height	3000

4.Function Diagram

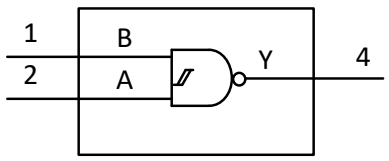

Fig 1. Logic symbol

Fig 2. IEC logic symbol

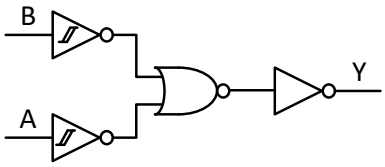

Fig 3. Logic diagram

5.Pinning Information

5.1. Pin map

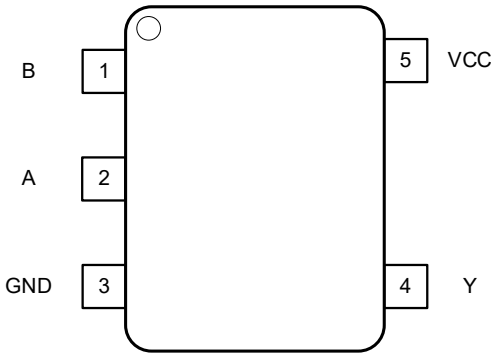

Fig 4. Top view pin configuration SOT23-5 and SOT353

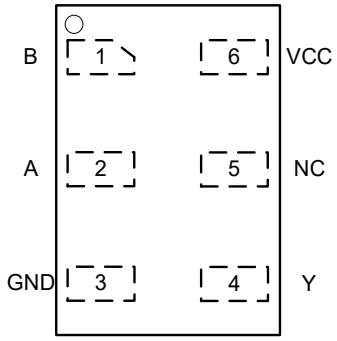

Fig 5. Top view pin configuration DFN6L

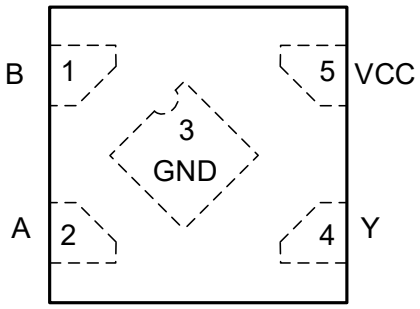

Fig 6. Top view pin configuration DFN4L

5.2. Pin description

Table 2. Pin description

Symbol	Pin		Description
	SOT23-5, SOT353 and DFN4L	DFN6L	
B	1	1	Data input
A	2	2	Data input
GND	3	3	Ground (0V)
Y	4	4	Data output
NC	-	5	Not connected
VCC	5	6	Supply voltage