EM74LVC1G57

Low-power configurable multiple function gate

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1. General Description

The EM74LVC1G57 is a configurable multiple function gate with Schmitt-trigger inputs. The device can be configured as any of the following logic functions AND, OR, NAND, NOR, XNOR, inverter and buffer; using the 3-bit input. All inputs can be connected directly to V_{CC} or GND. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and Benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- ±24 mA output drive (VCC = 3.0 V)
- CMOS low power dissipation
- Latch-up performance exceeds 100 mA
- Direct interface with TTL levels
- I_{OFF} circuitry provides partial Power-down mode operation
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 3B exceeds 8000 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options

3. Ordering Information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Quantity
EM74LVC1G57GV	VHYW	SOT23-6L	SOT23 package, 6 pins 2.92 mm × 1.6 mm; 1.25 mm (Max) height	3000
EM74LVC1G57GW	VHYW	SOT363	SOT363 package, 6 pins 2.1 mm × 1.25 mm; 1.1 mm (Max) height	3000

4. Function Diagram

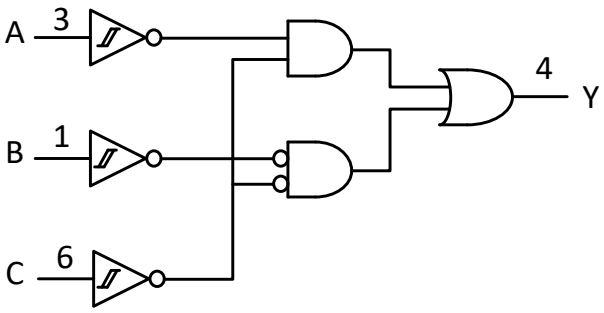

Fig. 1. Logic symbol

5. Pinning Information

5.1. Pinning

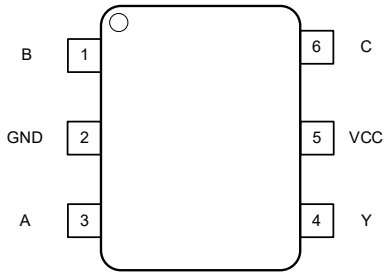

Fig. 2. Top view pin configuration SOT23-6 and SOT363

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
B	1	Data input
GND	2	Ground (0V)
A	3	Data input
Y	4	Data output
VCC	5	Supply voltage
C	6	Data input

6. Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

Input			Output
C	**B**	**A**	**Y**
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	H
H	H	H	H

6.1. Logic configurations

Table 4. Function selection table

Logic function	Figure
2-input AND	see Fig. 3
2-input AND with both inputs inverted	see Fig. 6
2-input NAND with inverted input	see Fig. 4 and Fig. 5
2-input OR with inverted input	see Fig. 4 and Fig. 5
2-input NOR	see Fig. 6
2-input NOR with both inputs inverted	see Fig. 3