

## 1. General Description

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The EM74HC126; EM74HCT126 is a quad buffer/line driver with 3-state outputs controlled by the output enable inputs (nOE). A LOW on nOE causes the outputs to assume a high impedance OFF-state. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

## 2. Features and Benefits

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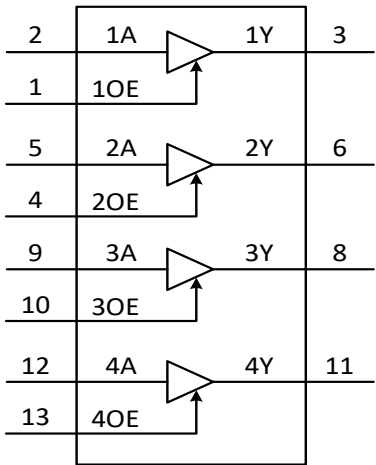
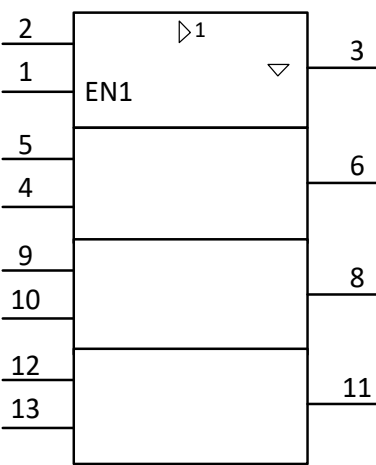
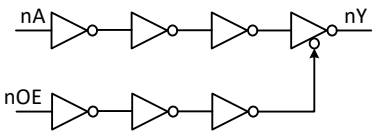
- Wide supply voltage range from 2.0 V to 6.0 V
- High noise immunity
- CMOS low power dissipation
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- Input levels:
  - For EM74HC126: CMOS level
  - For EM74HCT126: TTL level
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 3500 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options

### 3. Ordering Information

Table 1. Ordering information

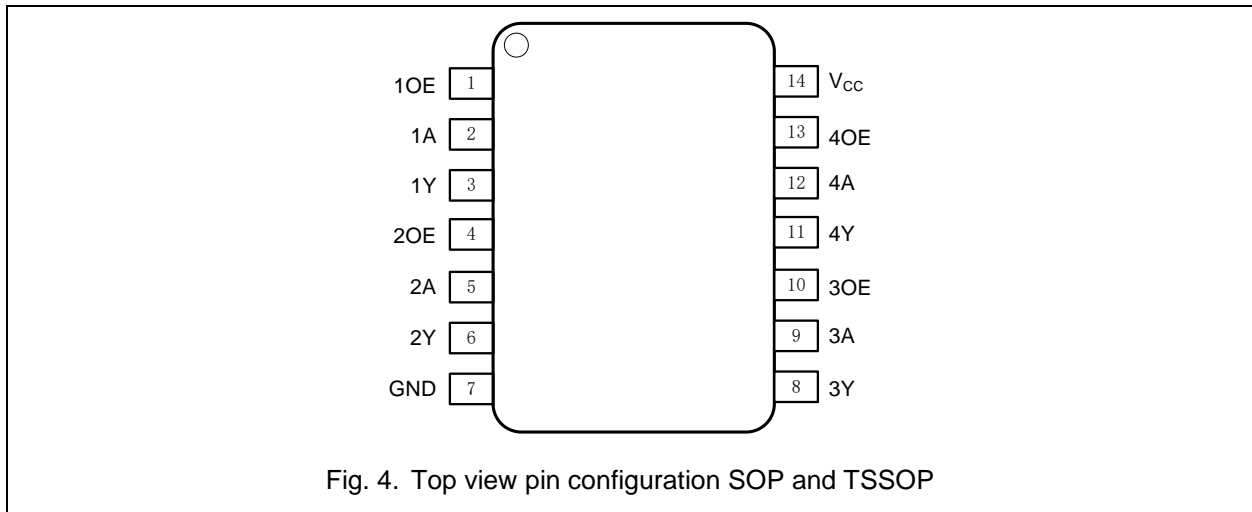
Type number	Package		
	Name	Description	Quantity
EM74HC126D	SOP-14L	plastic small outline package; 14 leads; body width 3.9 mm	3000
EM74HCT126D			
EM74HC126PW	TSSOP-14L	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	3000
EM74HCT126PW			

### 4. Function Diagram

 <p style="text-align: center;">Fig. 1. Logic symbol</p>	 <p style="text-align: center;">Fig. 2. IEC logic symbol</p>	 <p style="text-align: center;">Fig. 3. Logic diagram(one gate)</p>
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## 5. Pinning Information

### 5.1. Pinning



### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE, 3OE, 4OE	1, 4, 10, 13	Data enable input(active HIGH)
1A, 2A, 3A, 4A	2, 5, 9, 12	Data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	Data output
GND	7	Ground (0V)
V <sub>cc</sub>	14	Supply voltage

## 6. Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Output
nOE	nA	nY
H	L	L
H	H	H
L	X	Z