EMS3010

Isolated Daisy Chain Communication Interface

1.General Description

The EMS3010 provides bidirectional SPI communications between two isolated devices through a single twisted-pair connection. Each EMS3010 encodes logic states into signals that are transmitted across an isolation barrier to another EMS3010. The receiving EMS3010 decodes the transmission and drives the slave bus to the appropriate logic states. The isolation barrier can be bridged by a simple pulse transformer to achieve hundreds of volts of isolation.

The EMS3010 drives differential signals using matched source and sink currents, eliminating the requirement for a transformer center tap and reducing EMI. Precision window comparators in the receiver detect the differential signals. The drive currents and the comparator thresholds are set by a simple external resistor divider, allowing the system to be optimized for required cable lengths and desired signal-to-noise performance.

2.Features and Benefits

- **2.5Mbps EMiso (isolated daisy chain) Data Communications**
- **Simple Galvanic Isolation Using Standard Transformers**
- **Bidirectional Interface Over a Single Twisted Pair**
- **Supports Cable Lengths Up to 100 Meters**
- **Very Low EMI Susceptibility and Emissions**
- **Configurable for High Noise Immunity or Low Power**
- Requires No Software Changes in Most SPI Systems
- Ultralow, 3.6µA Idle Current
- Automatic Wake-Up Detection
- Operating Temperature Range: –40°C to 125°C
- 2.9V to 5.5V Power Supply
- Interfaces to All Logic from 1.7V to 5.5V
- Available in 16-Lead QFN and MSOP Packages

3.Applications

- Industrial Networking
- Battery Monitoring Systems
- Remote Sensors

4.Ordering information

Table 1 Ordering information

Type Number	Topside Marking	Package		
		Name	Description	Quantity
EMS3010UD	S3010 YYWW	QFN3x3-16L	QFN3x3 package;17 pin 3mm x 3mm; 0.8mm (Max) height	3000
EMS3010MS	S3010 YYWW	MSOP-16L	MSOP package;16 pin 4mm x 3mm; 1.1mm (Max) height	3000

5.Function diagram

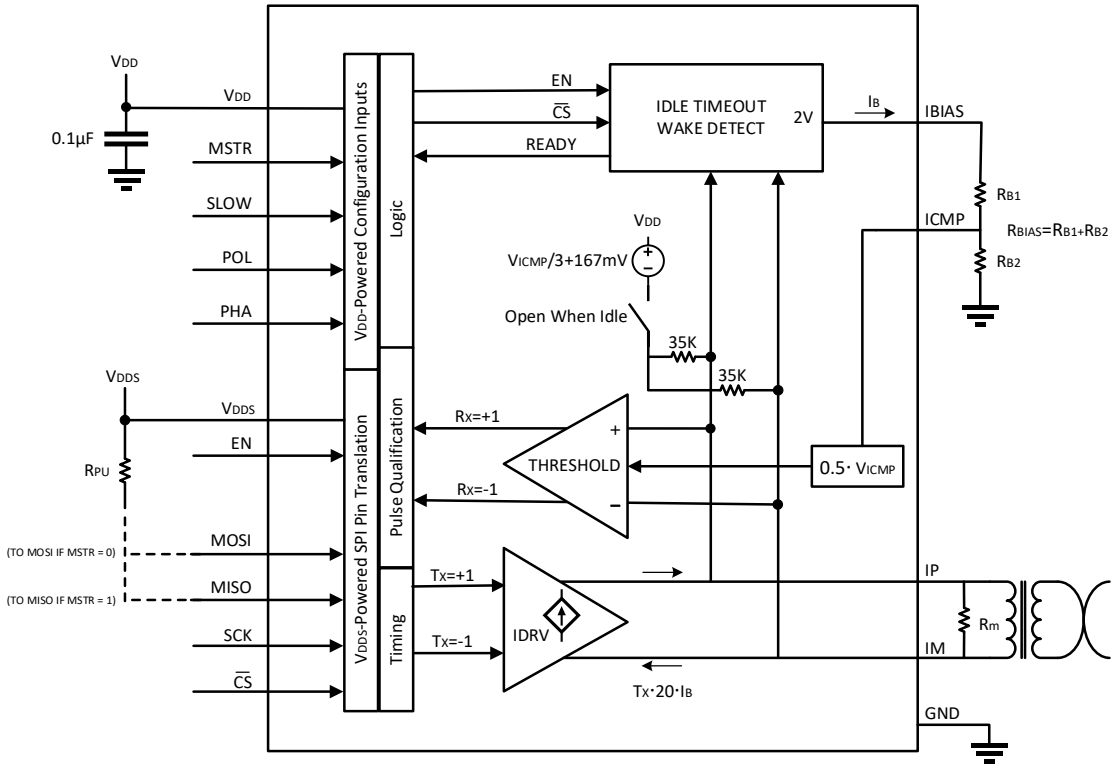


Fig 6. EMS3010 block diagram

6. Pinning information

6.1. Pin map

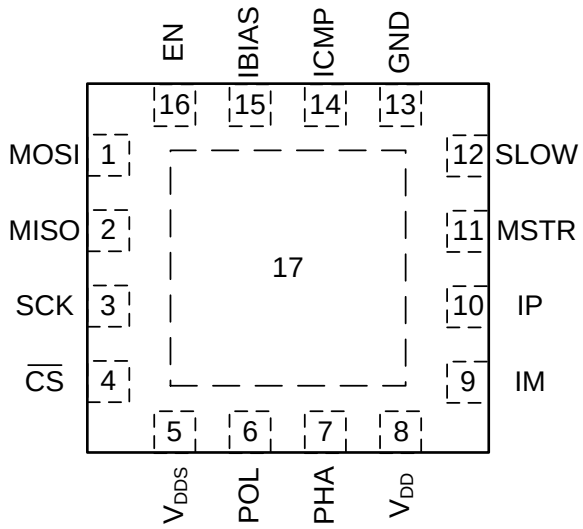


Fig 2. Top view pin configuration QFN

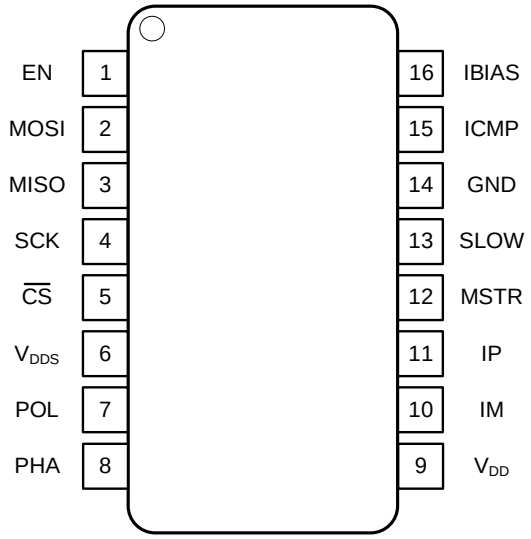


Fig 3. Top view pin configuration MSOP

6.2. Pin description

Table 2 Pin description

Pin Name	Pin Number		Description
	QFN	MSOP	
MOSI	1	2	SPI Master Out/Slave In Data. If connected on the master side of a SPI interface (MSTR pin high), this pin receives the data signal output from the master SPI controller. If connected on the slave side of the interface (MSTR pin low), this pin drives the data signal input to the slave SPI device. The output is open drain, so an external pull-up resistor to VDDS is required.
MISO	2	3	SPI Master In/Slave Out Data. If connected on the master side of a SPI interface (MSTR pin high), this pin drives the data signal input to the master SPI controller. If connected on the slave side of the interface (MSTR pin low), this pin receives the data signal output from the slave SPI device. The output is open drain, so an external pull-up resistor to VDDS is required.
SCK	3	4	SPI Clock Input/Output. If connected on the master side of the interface (MSTR pin high), this pin receives the clock signal from the master SPI controller. This input should not be pulled above V_{DDS}. If connected on the slave side of the interface (MSTR pin low), this pin outputs the clock signal to the slave device. The output driver is push-pull; no external pull-up resistor is needed.
$\overline{CS}$	4	5	SPI Chip Select Input/Output. If connected on the master side of the interface (MSTR pin high), this pin receives the chip select signal from the master SPI controller. This input should not be pulled above V_{DDS} . If connected on the slave side of the interface (MSTR pin low), this pin outputs the chip select signal to the slave device. The output driver is push-pull; no external pull-up resistor is needed.
V_{DDS}	5	6	SPI Input/Output Power Supply Input. The output drivers for the SCK and CS pins use the V_{DDS} input as their positive power supply. The input threshold voltages of SCK, CS, MOSI, MISO and EN are determined by V_{DDS}. May be tied to VDD or to a supply above or below V_{DD} to level shift the SPI I/O. If separate from V_{DD}, connect a bypass capacitor of at least 0.01µF directly between V_{DDS} and GND.
POL	6	7	SPI Clock Polarity Input. Tie to V_{DD} or GND. See Operation section for details.
PHA	7	8	SPI Clock Phase Input. Tie to V_{DD} or GND. See Operation section for details.
V_{DD}	8	9	Device Power Supply Input. Connect a bypass capacitor of at least 0.01µF directly between V_{DD} and GND.

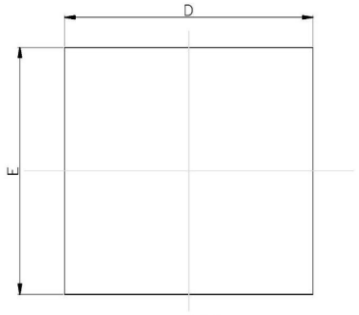
Table 3 Pin description (continued)

Pin Name	Pin Number		Description
	QFN	MSOP	
IM	9	10	Isolated Interface Minus Input/Output.
IP	10	11	Isolated Interface Plus Input/Output.
MSTR	11	12	Serial Interface Master/Slave Selector Input. Tie this pin to VDD if the device is on the master side of the isolated interface. Tie this pin to GND if the device is on the slave side of the isolated interface.
SLOW	12	13	Slow Interface Selection Input. For clock frequencies at or below 200kHz, or if slave devices cannot meet timing requirements, this pin should be tied to VDD. For clock frequencies above 200kHz, this pin should be tied to GND.
GND	13	14	Device Ground.
ICMP	14	15	Isolated Interface Comparator Voltage Threshold Set. Tie this pin to the resistor divider between IBIAS and GND to set the voltage threshold of the interface receiver comparators. The comparator thresholds are set to 1/2 the voltage on the ICMP pin.
IBIAS	15	16	Isolated Interface Current Bias. Tie IBIAS to GND through a resistor divider to set the interface output current level. When the device is enabled, this pin is approximately 2V. When transmitting pulses, the sink current on each of the IP and IM pins is set to 20 times the current sourced from pin IBIAS to GND. Limit the capacitance on the IBIAS pin to less than 50pF to maintain the stability of the feedback circuit regulating the IBIAS voltage.
EN	16	1	Device Enable Input. If high, this pin forces the EMS3010 to stay enabled, overriding the internal IDLE mode function. If low, the EMS3010 will go into IDLE mode after the CS pin has been high for 5.7ms (when MSTR pin is high) or after no signal on the IP/IM pins for 5.7ms (when MSTR pin is low). The EEMS3010will wake-up less than 8μs after $\overline{CS}$ falls (MSTR high) or after a signal is detected on IP/IM (MSTR low).
Exposed Pad	17	-	Exposed pad may be left open or connected to device GND.

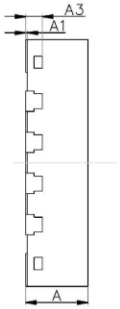
7.Package outline

QFN3x3-16L

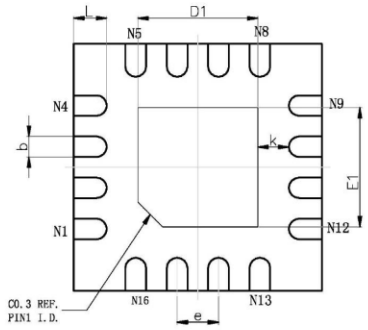
QFNWB3×3-16L-NB(P0.50T0.75) PACKAGE OUTLINE DIMENSIONS



TOP VIEW
[顶视图]



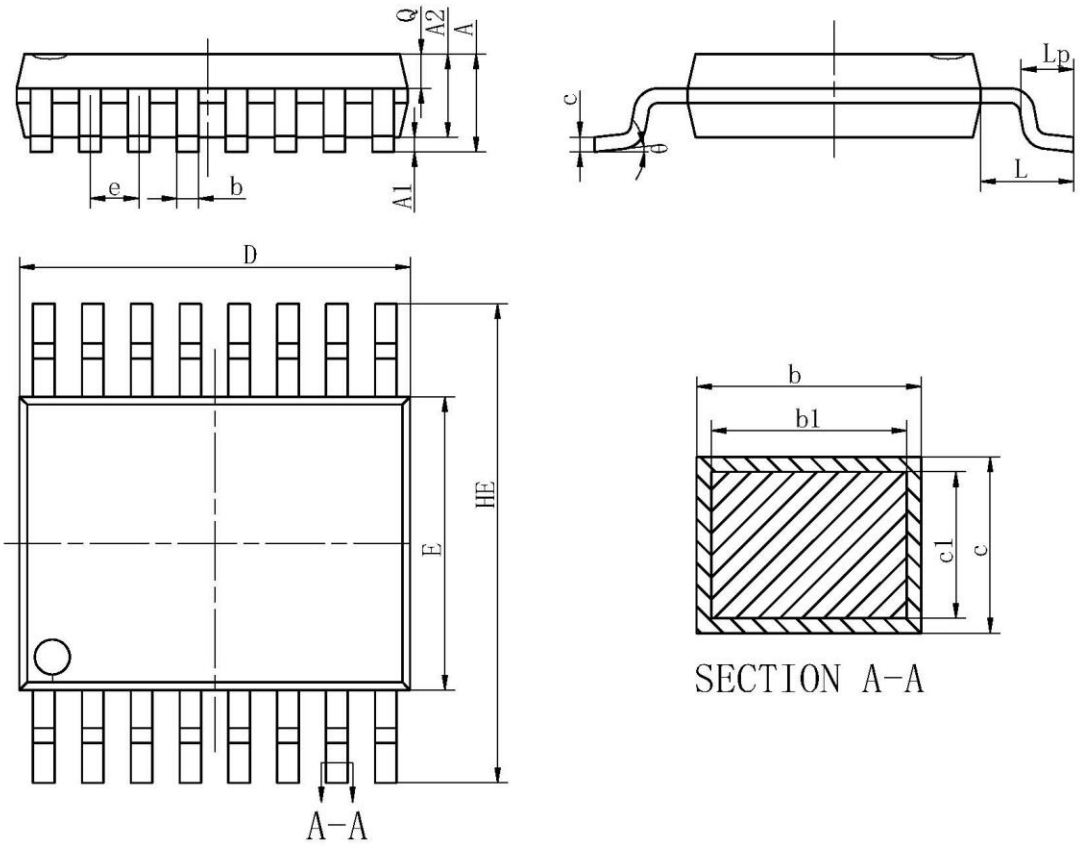
SIDE VIEW
[侧视图]



BOTTOM VIEW
[背视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	1.350	1.550	0.053	0.061
E1	1.350	1.550	0.053	0.061
k	0.375REF.		0.015REF.	
b	0.200	0.300	0.008	0.012
e	0.500BSC.		0.020BSC.	
L	0.300	0.500	0.012	0.020

MSOP-16L



SYMBOL	MIN(mm)	NOM(mm)	MAX(mm)
A	-	-	1.1
A1	0.05	-	0.15
A2	0.8	0.85	0.9
b	0.17	-	0.27
b1	-	0.2	-
c	0.13	-	0.23
c1	-	0.15	-
D	3.94	4.04	4.14
E	2.9	3	3.1
e	0.5BSC		
HE	4.7	4.9	5.1
L	-	0.95	-
Lp	0.4	-	0.7
Q	0.3	0.35	0.4
θ	0	-	6°

8. Abbreviations

Table 8 Abbreviations

Acronym	Description
CDM	Charged Device Model
HBM	Human Body Model

9. Revision history

Table 9 Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
EMS3010 Rev0.9	May 06, 2024	Draft datasheet		