EM74LVC74A

Dual D-type flip-flop with set and reset; positive-edge trigger

Product datasheet, Rev. 1.0 Aug 20, 2024

1.General Description

The EM74LVC74A is a dual edge triggered D-type flip-flop with individual data (nD) inputs, clock (nCP) inputs, set ($n\overline{SD}$) and ($n\overline{RD}$) inputs, and complementary nQ and $n\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the nQ output on the LOW-to-HIGH transition of the clock pulse. The nD inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2.Features and Benefits

- Wide supply voltage range from 1.2 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- CMOS low power dissipation
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C (2.7 V to 3.6 V)
  - JESD36 (4.5 V to 5.5 V)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 3A exceeds 6000 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options

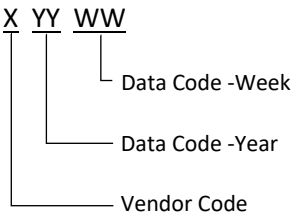
3.Ordering Information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Quantity
EM74LVC74AD	LVC74A XYYWW	SOP-14L	plastic small outline package; 14 leads; body width 3.9 mm	3000
EM74LVC74APW	LVC74A XYYWW	TSSOP-14L	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	3000

MARKING INFORMATION

NOTE: XYYWW = Vendor Code and Data Code.



4. Function Diagram

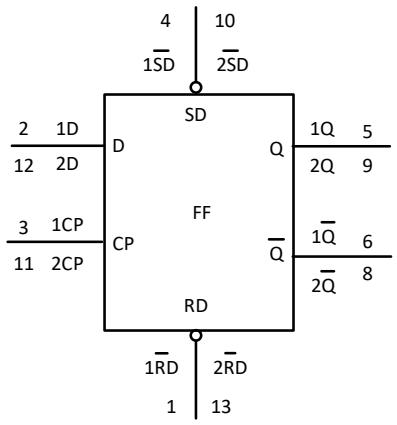


Fig. 1. Logic symbol

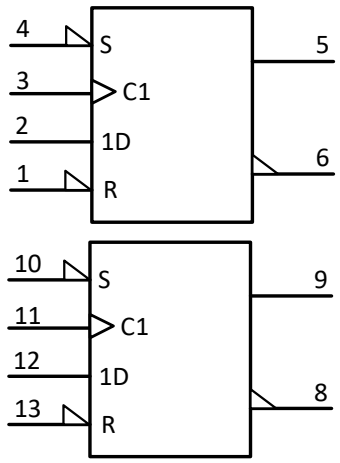


Fig. 2. IEC logic symbol

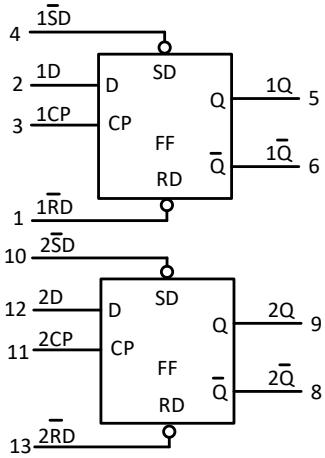


Fig. 3. Functional diagram

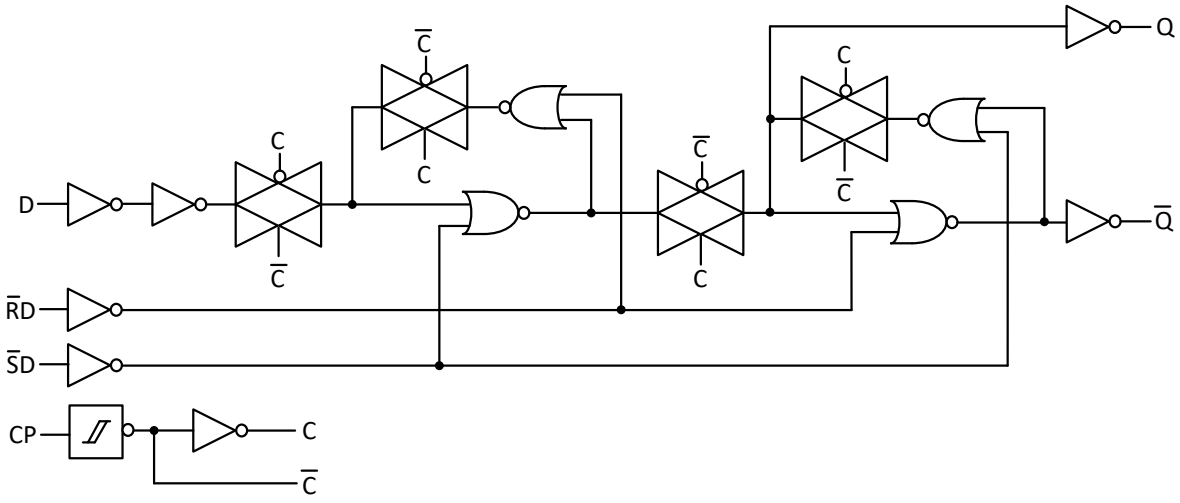


Fig. 4. Logic diagram for one flip-flop

5.Pinning Information

5.1. Pin map

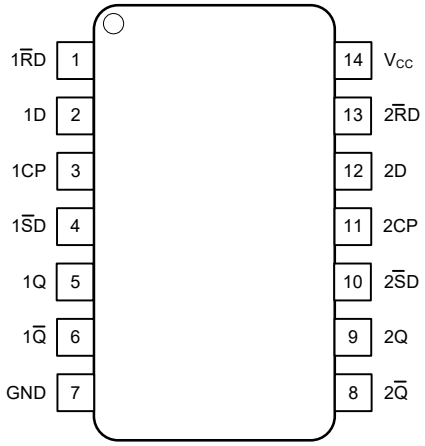


Fig. 5. Top view pin configuration SOP and TSSOP

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1$\overline{R}$D, 2$\overline{R}$D	1, 13	asynchronous reset-direct input (active LOW)
1D, 2D	2, 12	data input
1CP, 2CP	3, 11	clock input (LOW-to-HIGH, edge-triggered)
1$\overline{S}$D, 2$\overline{S}$D	4, 10	asynchronous set-direct input (active LOW)
1Q, 2Q	5, 9	true output
1$\overline{Q}$, 2$\overline{Q}$	6, 8	complement output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6.Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input				Output	
$n\overline{SD}$	$n\overline{RD}$	nCP	nD	nQ	$n\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

↑ = LOW-to-HIGH transition; Q_{n+1} = state after the next LOW-to-HIGH CP transition.

Input				Output	
$n\overline{SD}$	$n\overline{RD}$	nCP	nD	nQ_{n+1}	$n\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

7.Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 5. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50		mA
V_I	input voltage	[1]	-0.5	6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		±50	mA
V_O	output voltage	Active mode; [1]	-0.5	V_{CC} + 0.5	V
		Power-down mode; V_{CC} = 0 V [1]	-0.5	6.5	V
I_O	output current	V_O = 0 V to V_{CC}		±50	mA
I_{CC}	supply current			100	mA
I_{GND}	ground current		-100		mA
P_{tot}	total power dissipation	T_{amb} = -40 °C to + 125 °C		500	mW
T_{stg}	storage temperature		-65	150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 6. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	for maximum speed performance	1.65	5.5	V
		functional	1.2		V
V_I	input voltage		0	5.5	V
V_O	output voltage	Active mode;	0	V_{CC}	V
		Power-down mode; V_{CC} = 0 V		5.5	V
T_{amb}	ambient temperature		-40	125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	0	10	ns/V

9. Static Characteristics

Table 7. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	1.08			1.08		V
		V_{CC} = 1.65 V to 1.95 V	0.65V_{CC}			0.65V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7			1.7		V
		V_{CC} = 2.7 V to 3.6 V	2.0			2.0		V
		V_{CC} = 4.5 V to 5.5 V	0.7V_{CC}			0.7V_{CC}		V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V			0.12		0.12	V
		V_{CC} = 1.65 V to 1.95 V			0.35V_{CC}		0.35V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V			0.7		0.7	V
		V_{CC} = 2.7 V to 3.6 V			0.8		0.8	V
		V_{CC} = 4.5 V to 5.5 V			0.3V_{CC}		0.3V_{CC}	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -100 µA; V_{CC} = 1.65 V to 5.5 V	V_{CC} - 0.1			V_{CC} - 0.1		V
		I_O = -4 mA; V_{CC} = 1.65 V	1.2			1.05		V
		I_O = -8 mA; V_{CC} = 2.3 V	1.9			1.7		V

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{OH}	HIGH-level output voltage	I_O = -12 mA; V_{CC} = 2.7 V	2.2			2.05		V
		I_O = -24 mA; V_{CC} = 3.0 V	2.4			2.25		V
		I_O = -32 mA; V_{CC} = 4.5 V	3.8			3.5		V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 100 µA; V_{CC} = 1.65 V to 5.5 V			0.10		0.10	V
		I_O = 4 mA; V_{CC} = 1.65 V			0.45		0.65	V
		I_O = 8 mA; V_{CC} = 2.3 V			0.30		0.45	V
		I_O = 12 mA; V_{CC} = 2.7 V			0.40		0.60	V
		I_O = 24 mA; V_{CC} = 3.0 V			0.55		0.80	V
		I_O = 32 mA; V_{CC} = 4.5 V			0.55		0.80	V
I_I	input leakage current	V_I = 5.5 V or GND ; V_{CC} = 0 V to 5.5 V		±0.1	±5		±20	µA
I_{CC}	supply current	V_I = 5.5V or GND ; I_O = 0 A ; V_{CC} = 1.65V to 5.5V		0.01	10		40	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0 V ; V_I or V_O = 5.5 V		±0.1	±10		±20	µA
ΔI_{CC}	additional supply current	per input pin ; V_{CC} = 2.3 V to 5.5 V ; V_I = V_{CC} -0.6 V ; I_O = 0 A		0.5	500		5000	µA
C_I	input capacitance	V_{CC} = 3.3V ; V_I = GND to V_{CC}		4				pF

[1]All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25℃.

10. Dynamic Characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nCP to nQ, n$\overline{Q}$; see Fig. 6 [2]						
		V_{CC} = 1.65 V to 1.95 V	1.0		22	1.0	23	ns
		V_{CC} = 2.3 V to 2.7 V	1.0		12	1.8	13	ns
		V_{CC} = 3.0 V to 3.6 V	1.0		9	1.0	10	ns
		V_{CC} = 4.5 V to 5.5 V	1.0		6	1.0	7	ns
		n$\overline{SD}$ to nQ, n$\overline{Q}$; see Fig. 7 [2]						
		V_{CC} = 1.65 V to 1.95 V	1.0		24	0.5	25	ns
		V_{CC} = 2.3 V to 2.7 V	1.0		12	1.0	13	ns
		V_{CC} = 3.0 V to 3.6 V	1.0		8.5	1.0	9	ns
		V_{CC} = 4.5 V to 5.5 V	1.0		6.5	1.0	7	ns
		n$\overline{RD}$ to nQ, n$\overline{Q}$; see Fig. 7 [2]						
		V_{CC} = 1.65 V to 1.95 V	1.0		24.5	0.5	25	ns
		V_{CC} = 2.3 V to 2.7 V	1.0		14	1.0	15	ns
		V_{CC} = 3.0 V to 3.6 V	1.0		9	1.0	10	ns
		V_{CC} = 4.5 V to 5.5 V	1.0		6	1.0	7	ns
t_W	pulse width	clock HIGH or LOW; see Fig. 6						
		V_{CC} = 1.65 V to 1.95 V	5.0			5.0		ns
		V_{CC} = 2.3 V to 2.7 V	4.0			4.0		ns
		V_{CC} = 3.0 V to 3.6 V	3.3			4.5		ns
		V_{CC} = 4.5 V to 5.5 V	3.3			4.5		ns
		set or reset LOW; see Fig. 7						
		V_{CC} = 1.65 V to 1.95 V	5.0			5.0		ns
		V_{CC} = 2.3 V to 2.7 V	4.0			4.0		ns
		V_{CC} = 3.0 V to 3.6 V	3.3			4.5		ns
		V_{CC} = 4.5 V to 5.5 V	3.3			4.5		ns
t_{rec}	recovery time	set or reset; see Fig. 7						
		V_{CC} = 1.65 V to 1.95 V	1.5			1.5		ns
		V_{CC} = 2.3 V to 2.7 V	1.5			1.5		ns
		V_{CC} = 3.0 V to 3.6 V	1.0			1.0		ns
		V_{CC} = 4.5 V to 5.5 V	1.0			1.0		ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{su}	set-up time	nD to nCP; see Fig. 6						
		V_{CC} = 1.65 V to 1.95 V	3.0			3.0		ns
		V_{CC} = 2.3 V to 2.7 V	2.5			2.5		ns
		V_{CC} = 3.0 V to 3.6 V	2.0			2.0		ns
		V_{CC} = 4.5 V to 5.5 V	2.0			2.0		ns
t_h	hold time	nD to nCP; see Fig. 6						
		V_{CC} = 1.65 V to 1.95 V	2.0			2.0		ns
		V_{CC} = 2.3 V to 2.7 V	1.5			1.5		ns
		V_{CC} = 3.0 V to 3.6 V	1.0			1.0		ns
		V_{CC} = 4.5 V to 5.5 V	1.0			1.0		ns
f_{max}	maximum frequency	nCP; see Fig. 6						
		V_{CC} = 1.65 V to 1.95 V	35			30		MHz
		V_{CC} = 2.3 V to 2.7 V	70			65		MHz
		V_{CC} = 3.0 V to 3.6 V	100			90		MHz
		V_{CC} = 4.5 V to 5.5 V	150			130		MHz
$t_{sk(o)}$	output skew time	V_{CC} = 3.0 V to 3.6 V [3]			1.0		1.5	ns
C_{PD}	power dissipation capacitance	per flip-flop ; V_I = GND to V_{CC} [4]						
		V_{CC} = 1.65 V to 1.95 V		12				pF
		V_{CC} = 2.3 V to 2.7 V		13				pF
		V_{CC} = 3.0 V to 3.6 V		14				pF
		V_{CC} = 4.5 V to 5.5 V		15				pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

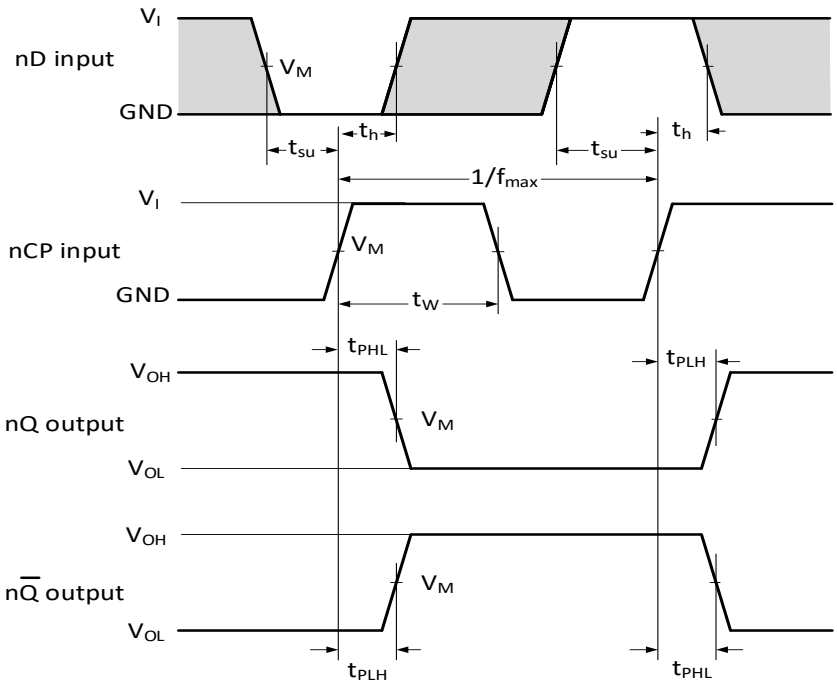
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

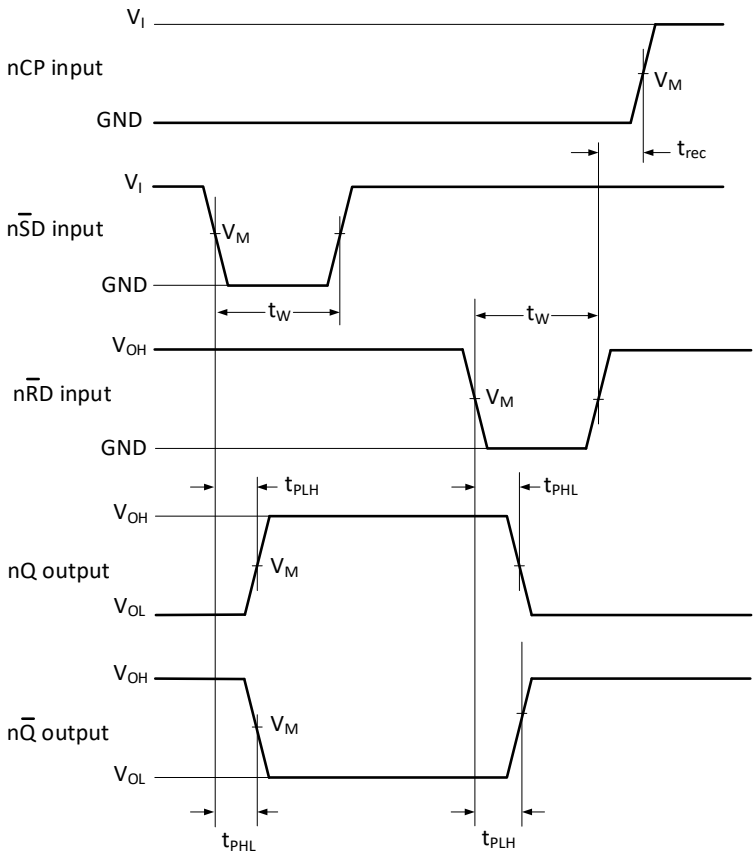
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



The shaded areas indicate when the input is permitted to change for predictable output performance.
Measurement points are given in Table 9.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. The clock input (nCP) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nD to nCP set-up, the nCP to nD hold times, and the maximum frequency



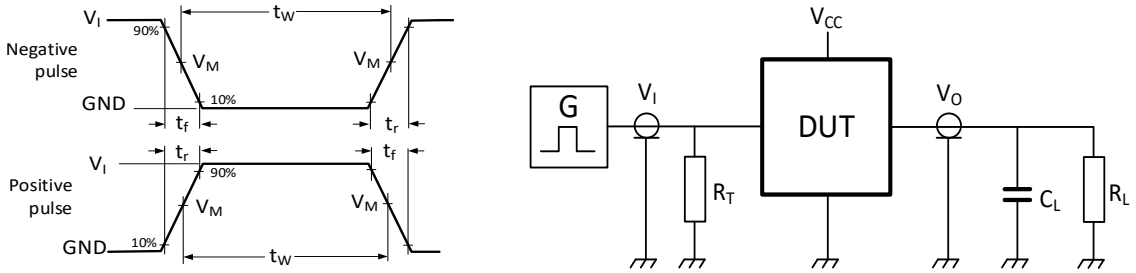
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. The set ($n\overline{SD}$) and reset ($n\overline{RD}$) input to output (nQ, $n\overline{Q}$) propagation delays, the set and reset pulse widths,and the $n\overline{RD}$ to nCP recovery time

Table 9. Measurement points

Supply voltage	Input		Output
V_{CC}	V_I	V_M	V_M
1.2 V	V_{CC}	0.5 x V_{CC}	0.5 x V_{CC}
1.65 V to 1.95 V	V_{CC}	0.5 x V_{CC}	0.5 x V_{CC}
2.3 V to 2.7 V	V_{CC}	0.5 x V_{CC}	0.5 x V_{CC}
3.0 V to 3.6 V	3.0 V	1.5 V	1.5 V
4.5 V to 5.5 V	V_{CC}	0.5 x V_{CC}	0.5 x V_{CC}



Test data is given in Table 10.
Definitions for test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to output impedance Zo of the pulse generator.

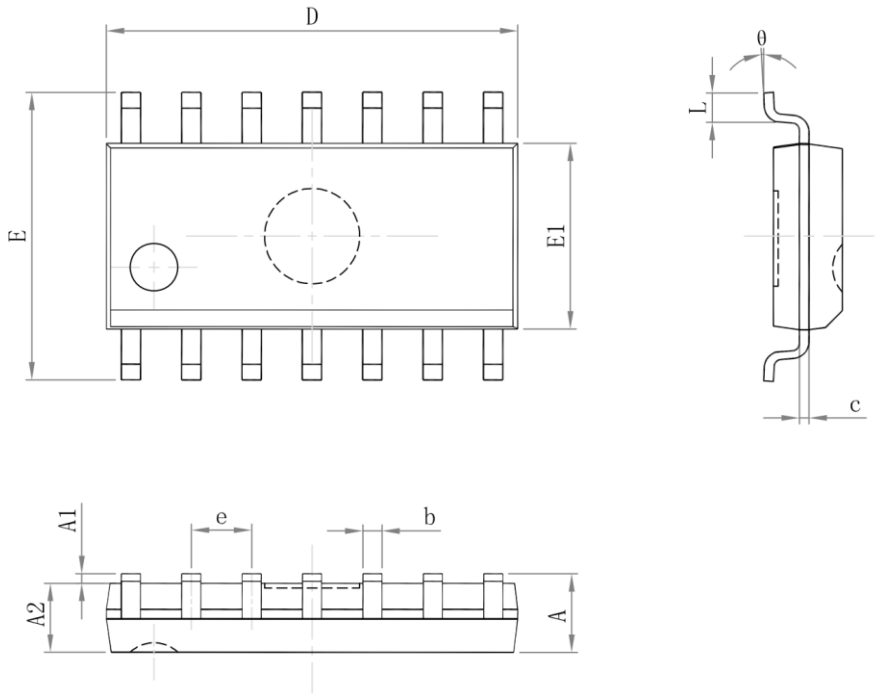
Fig. 8. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load	
V_{CC}	V_I	$t_r = t_f$	C_L	R_L
1.2 V	V_{CC}	≤ 2.0 ns	15 pF	500 Ω
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	15 pF	500 Ω
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	15 pF	500 Ω
3.0 V to 3.6 V	3 V	≤ 2.0 ns	15 pF	500 Ω
4.5 V to 5.5 V	V_{CC}	≤ 2.0 ns	15 pF	500 Ω

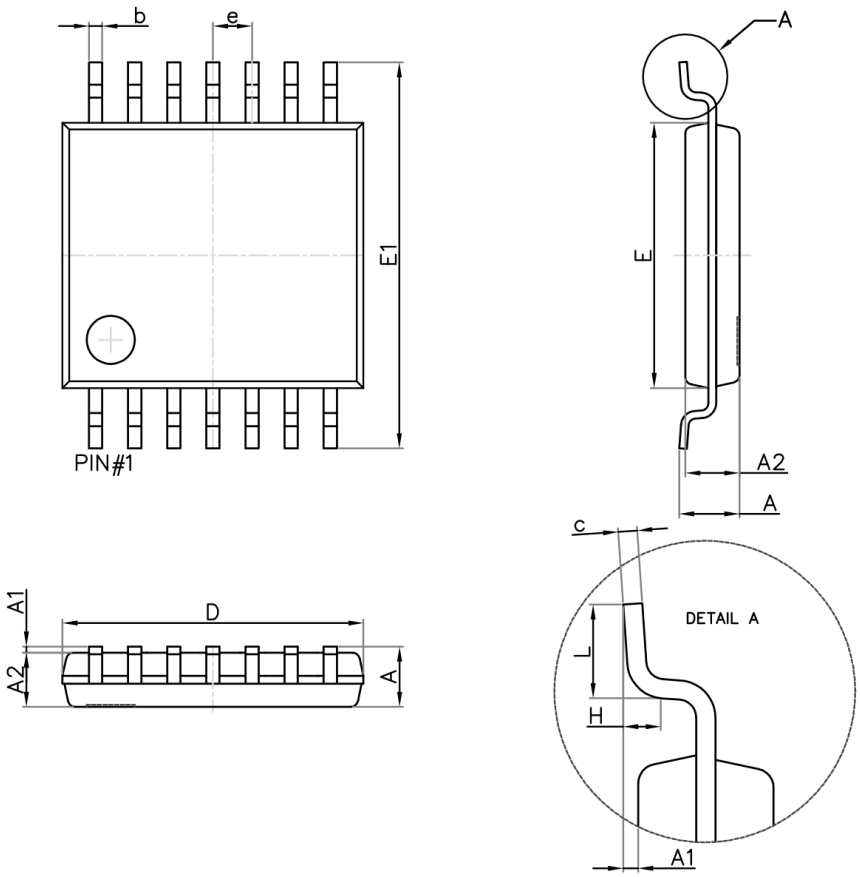
11. Package Outline

SOP-14L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	— —	1.750	— —	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	— —	0.049	— —
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

TSSOP-14L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
D	4.900	5.100	0.193	0.201
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A	—	1.200	—	0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model
TTL	Transistor-Transistor Logic

13. Revision History

Table 12. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
EM74LVC74A Rev. 1.0	Aug 20, 2024	datasheet		