EM74AUP1G11

Low-power 3-input AND gate

Product datasheet, Rev. 1.0 Oct 18, 2025

1. General Description

The EM74AUP1G11 is a single 3-input AND gate. Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times. This device ensures very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V. This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and Benefits

- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- Low static power consumption; I_{CC} = 0.9 µA (maximum)
- Low noise overshoot and undershoot < 10 % of V_{CC}
- Overvoltage tolerant inputs to 3.6 V
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 100 mA
- Complies with JEDEC standard:
  - JESD8-12 (0.8 V to 1.3 V)
  - JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-B (2.7 V to 3.6 V)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 3A exceeds 5000 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 1000 V
- Multiple package options

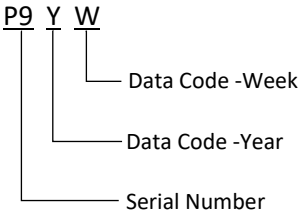
3. Ordering Information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Quantity
EM74AUP1G11GV	P9YW	SOT23-6L	SOT23 package, 6 pins 2.92 mm × 1.6 mm; 1.25 mm (Max) height	3000
EM74AUP1G11GW	P9YW	SOT363	SOT363 package, 6 pins 2.1 mm × 1.25 mm; 1.1 mm (Max) height	3000
EM74AUP1G11GS	P9	DFN1x1-6L	DFN1×1 package, 6 pins 1 mm × 1 mm; 0.42 mm (Max) height	3000
EM74AUP1G11GM	P9YW	DFN1x1.45-6L	DFN1.45×1 package, 6 pins 1.45 mm × 1 mm; 0.6 mm (Max) height	3000

MARKING INFORMATION

NOTE: YW = Data Code.



4. Function Diagram

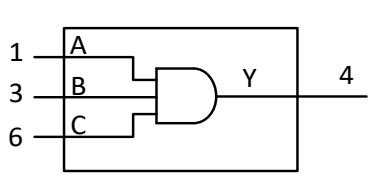


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

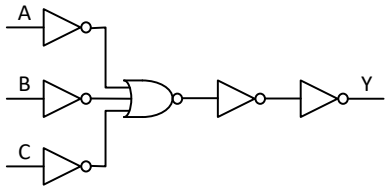


Fig. 3. Logic diagram

5.Pinning Information

5.1. Pinning

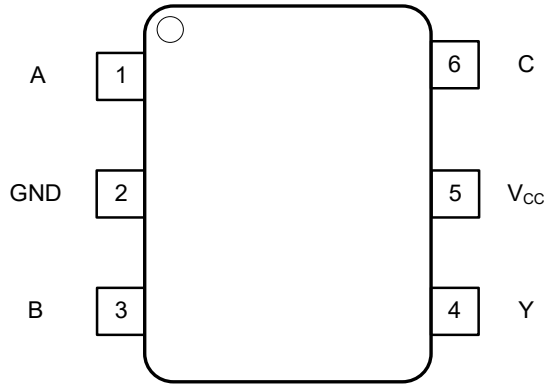


Fig. 4. Top view pin configuration SOT23-6 and SOT363

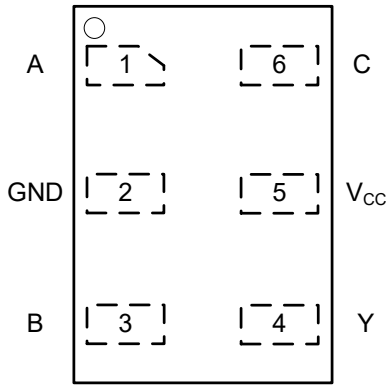


Fig. 5. Top view pin configuration DFN6L

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
A	1	Data input
GND	2	Ground (0V)
B	3	Data input
Y	4	Data output
V_{CC}	5	Supply voltage
C	6	Data input

6.Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input			Output
A	**B**	**C**	**Y**
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

7.Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 5. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	4.6	V
I_{IK}	input clamping current	$V_I < 0$ V	-50		mA
V_I	input voltage	[1]	-0.5	4.6	V
I_{OK}	output clamping current	$V_O < 0$ V	-50		mA
V_O	output voltage	Active mode [1]	-0.5	4.6	V
		Power-down mode; V_{CC} = 0 V [1]	-0.5	4.6	V
I_O	output current	V_O = 0 V to V_{CC}		±20	mA
I_{CC}	supply current			50	mA
I_{GND}	ground current		-50		mA
P_{tot}	total power dissipation	T_{amb} = -40 °C to + 125 °C		250	mW
T_{stg}	storage temperature		-65	150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 6. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		0.8		3.6	V
V_I	input voltage		0		3.6	V
V_O	output voltage	Active mode	0		V_{CC}	V
		Power-down mode; V_{CC} = 0V	0		3.6	V
T_{amb}	ambient temperature		-40		125	°C
Δt/ΔV	Input transition rise and fall rate	V_{CC} = 0.8 V to 3.6 V			200	ns/V

9.Static Characteristics

Table 7. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 0.8 V	0.7V_{CC}			0.75V_{CC}		V
		V_{CC} = 0.9 V to 1.95 V	0.65V_{CC}			0.7V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.6			1.6		V
		V_{CC} = 3.0 V to 3.6 V	2.0			2.0		V
V_{IL}	LOW-level input voltage	V_{CC} = 0.8 V			0.3V_{CC}		0.25V_{CC}	V
		V_{CC} = 0.9 V to 1.95 V			0.35V_{CC}		0.3V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V			0.7		0.7	V
		V_{CC} = 3.0 V to 3.6 V			0.9		0.9	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -20µA; V_{CC} = 0.8 V to 3.6 V	V_{CC} - 0.1			V_{CC} - 0.11		V
		I_O = -1.1 mA; V_{CC} = 1.1 V	0.75V_{CC}			0.6V_{CC}		V
		I_O = -1.7 mA; V_{CC} = 1.4 V	1.03			0.93		V
		I_O = -1.9 mA; V_{CC} = 1.65 V	1.30			1.17		V
		I_O = -2.3 mA; V_{CC} = 2.3 V	1.97			1.77		V
		I_O = -3.1 mA; V_{CC} = 2.3 V	1.85			1.67		V
		I_O = -2.7 mA; V_{CC} = 3.0 V	2.67			2.40		V
		I_O = -4.0 mA; V_{CC} = 3.0 V	2.55			2.30		V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 20µA; V_{CC} = 0.8 V to 3.6 V			0.10		0.11	V
		I_O = 1.1 mA; V_{CC} = 1.1 V			0.3V_{CC}		0.33V_{CC}	V
		I_O = 1.7 mA; V_{CC} = 1.4 V			0.37		0.41	V
		I_O = 1.9 mA; V_{CC} = 1.65 V			0.35		0.39	V
		I_O = 2.3 mA; V_{CC} = 2.3 V			0.33		0.36	V
		I_O = 3.1 mA; V_{CC} = 2.3 V			0.45		0.50	V
		I_O = 2.7 mA; V_{CC} = 3.0 V			0.33		0.36	V
		I_O = 4.0 mA; V_{CC} = 3.0 V			0.45		0.50	V

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
I_I	Input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V			±0.5		±0.75	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V ; V_I or V_O = 0 V to 3.6 V			±0.5		±0.75	µA
ΔI_{OFF}	additional power-off leakage current	V_{CC} = 0 V to 0.2 V ; V_I or V_O = 0V to 3.6 V			±0.6		±0.75	µA
I_{CC}	supply current	V_I = V_{CC} or GND ; I_O = 0 A ; V_{CC} = 0.8 V to 3.6 V			0.9		1.4	µA
ΔI_{CC}	additional supply current	per pin ; V_{CC} = 3.3 V ; V_I = V_{CC} - 0.6 V ; I_O = 0 A			50		75	µA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V						
		Pin A		2.0				pF
		Pin B, C		3.0				pF
C_O	output capacitance	V_{CC} = 0 V		4.1				pF

[1]All typical values are measured at T_{amb} = 25℃.

10. Dynamic Characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
C_L = 5 pF								
t_{pd}	propagation delay	A, B and C to Y; see Fig. 6 [2]						
		V_{CC} = 0.8 V		69.7				ns
		V_{CC} = 1.1 V to 1.3 V	2.8	9.5	19.2	2.8	20.2	ns
		V_{CC} = 1.4 V to 1.6 V	2.2	6	9.4	2.2	11.4	ns
		V_{CC} = 1.65 V to 1.95 V	1.8	3.9	7.4	1.8	8.6	ns
		V_{CC} = 2.3 V to 2.7 V	1.4	2.7	4.3	1.4	5.1	ns
		V_{CC} = 3.0 V to 3.6 V	1.2	2.2	3.4	1.2	4.4	ns
C_L = 10 pF								
t_{pd}	propagation delay	A, B and C to Y; see Fig. 6 [2]						
		V_{CC} = 0.8 V		72.5				ns
		V_{CC} = 1.1 V to 1.3 V	3.3	11	20.7	3.3	21.5	ns
		V_{CC} = 1.4 V to 1.6 V	2.6	6.8	10.2	2.6	12.2	ns
		V_{CC} = 1.65 V to 1.95 V	2.1	4.4	7.9	2.1	9.0	ns
		V_{CC} = 2.3 V to 2.7 V	1.7	3	4.6	1.7	5.4	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	2.5	3.7	1.5	4.5	ns
C_L = 15 pF								
t_{pd}	propagation delay	A, B and C to Y; see Fig. 6 [2]						
		V_{CC} = 0.8 V		78.4				ns
		V_{CC} = 1.1 V to 1.3 V	3.6	12.5	22.2	3.6	22.8	ns
		V_{CC} = 1.4 V to 1.6 V	2.9	7.6	11.0	2.9	13.0	ns
		V_{CC} = 1.65 V to 1.95 V	2.4	4.9	8.4	2.4	9.4	ns
		V_{CC} = 2.3 V to 2.7 V	2.0	3.3	4.9	2.0	5.7	ns
		V_{CC} = 3.0 V to 3.6 V	1.8	2.8	4.0	1.8	4.6	ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
C_L = 30 pF								
t_{pd}	propagation delay	A, B and C to Y; see Fig. 6 [2]						
		V_{CC} = 0.8 V		91.3				ns
		V_{CC} = 1.1 V to 1.3 V	4.8	16.1	26.6	4.8	26.1	ns
		V_{CC} = 1.4 V to 1.6 V	3.8	9.6	13.4	3.8	14.0	ns
		V_{CC} = 1.65 V to 1.95 V	3.2	6.1	10.1	3.2	10.6	ns
		V_{CC} = 2.3 V to 2.7 V	2.8	4.1	5.7	2.8	6.3	ns
		V_{CC} = 3.0 V to 3.6 V	2.5	3.1	4.9	2.5	5.2	ns
C_L = 5 pF, 10 pF, 15 pF and 30 pF								
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC} [3]						
		V_{CC} = 0.8 V		5.3				pF
		V_{CC} = 1.1 V to 1.3 V		5.5				pF
		V_{CC} = 1.4 V to 1.6 V		5.6				pF
		V_{CC} = 1.65 V to 1.95 V		5.8				pF
		V_{CC} = 2.3 V to 2.7 V		6.1				pF
		V_{CC} = 3.0 V to 3.6 V		7.7				pF

[1] Typical values are measured at norminal V_{CC} and at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

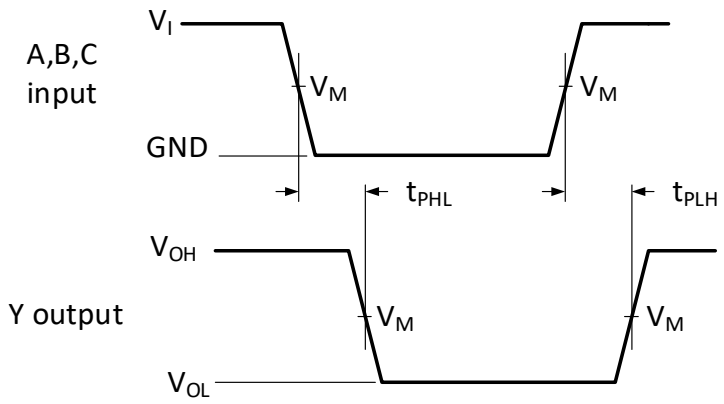
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit

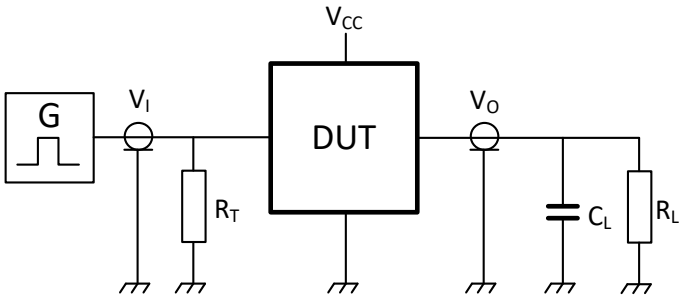


Measurement points are given in Table 9.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. Input A, B and C to output Y propagation delays

Table 9. Measurement points

Supply Voltage	Input	Output
V_{CC}	V_M	V_M
0.8 V to 3.6 V	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in Table 10.
Definitions for test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

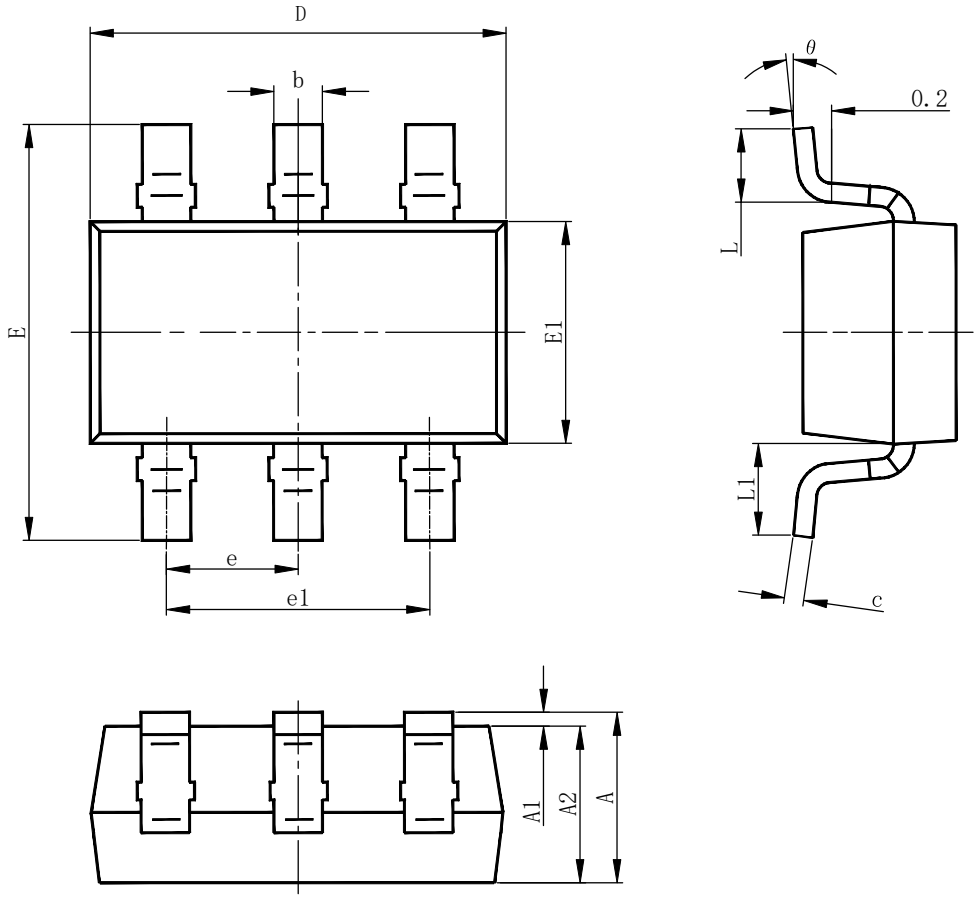
Fig. 7. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	**Input**		**Load**	
V_{CC}	**V_I**	**$t_r = t_f$**	**C_L**	**R_L**
0.8 V to 3.6 V	V_{CC}	≤ 2.0 ns	5 pF, 10 pF, 15 pF and 30 pF	1 MΩ

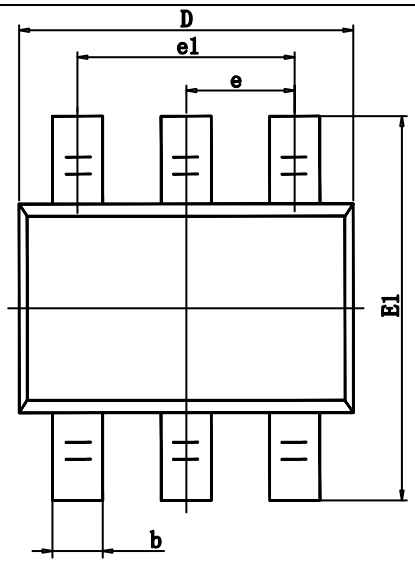
11. Package Outline

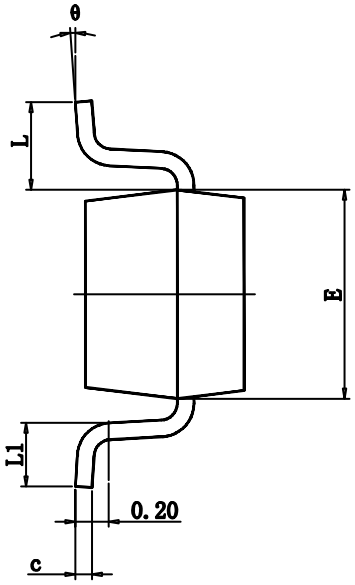
SOT23-6L

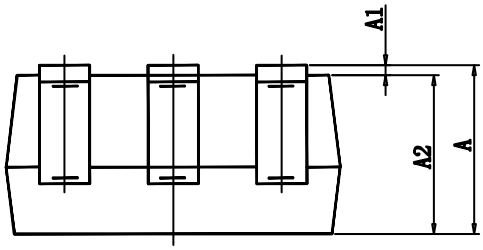


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
L1	0.600REF.		0.024REF.	
θ	0°	8°	0°	8°

SOT363

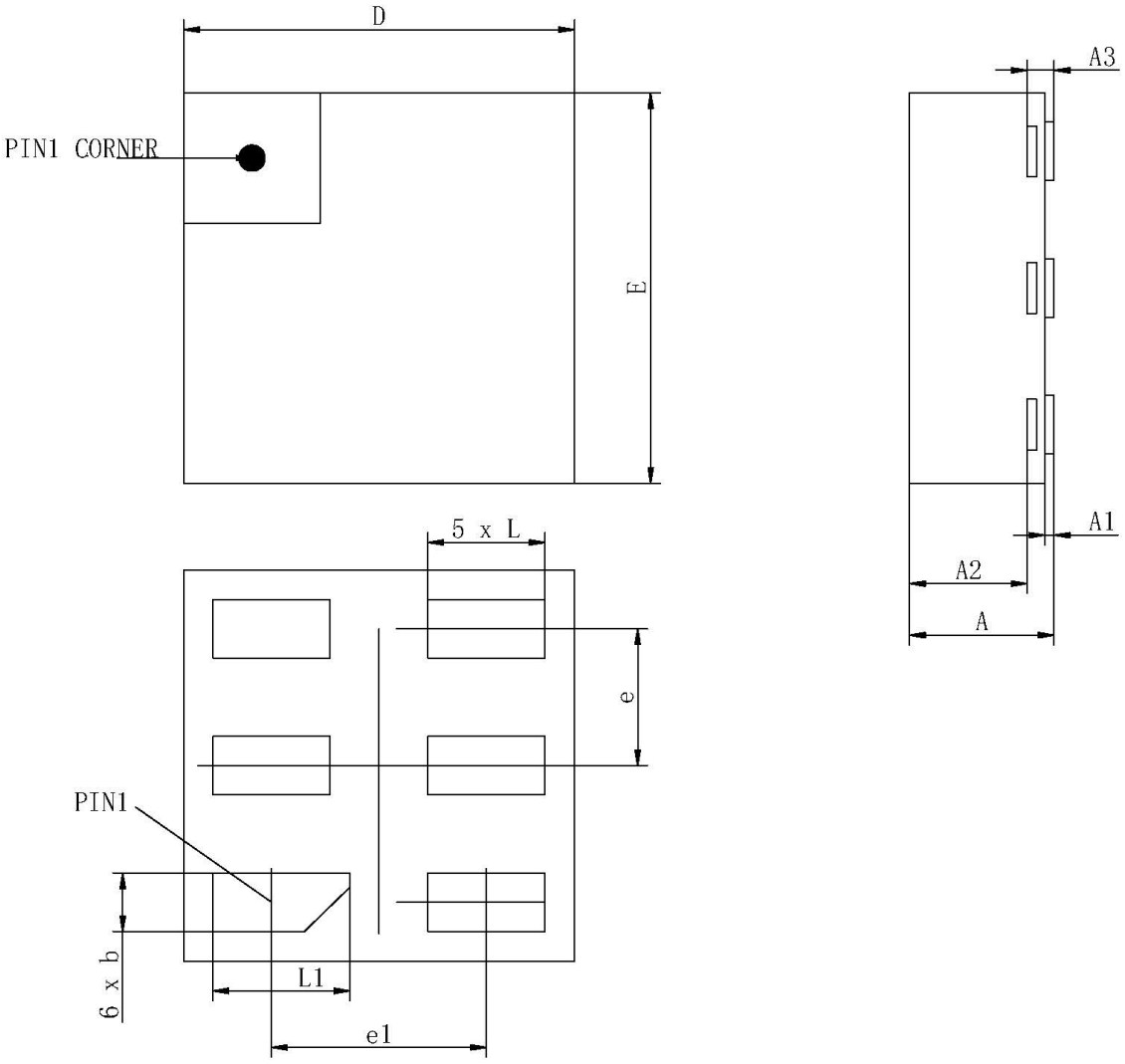






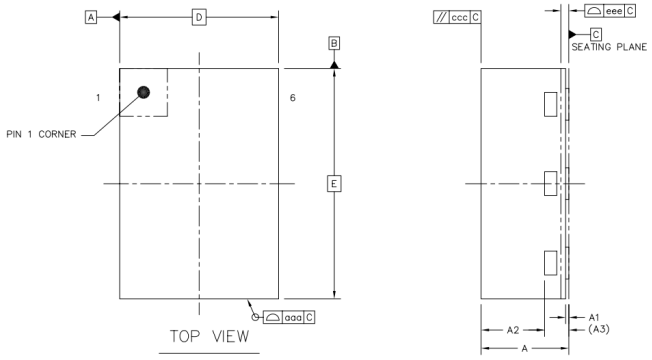
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.110	0.175	0.004	0.007
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650 TYP.		0.026 TYP.	
e1	1.200	1.400	0.047	0.055
L	0.525 REF.		0.021 REF.	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

DFN1x1-6L



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.32	0.37	0.42
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.27	---
L/F THICKNESS		A3		0.102 REF	
BODY SIZE	X	D		1.00 BSC	
	Y	E		1.00 BSC	
LEAD WIDTH		b	0.10	0.15	0.20
LEAD PITCH		e		0.35 BSC	
		e1		0.55 BSC	
LEAD LENGTH		L	0.25	0.30	0.35
		L1	0.30	0.35	0.40

DFN1x1.45-6L



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3		0.152 REF	
LEAD WDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		1 BSC	
	Y	E		1.45 BSC	
LEAD PITCH		e		0.5 BSC	
LEAD LENGTH		L	0.25	0.3	0.35
		L1		0.05 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.05	
LEAD OFFSET		bbb		0.1	

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING;
4.FINISH: Cu/EP •Sn8~20s

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model
TTL	Transistor-Transistor Logic

13. Revision History

Table 12. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
EM74AUP1G11 Rev. 1.0	Oct 18, 2025	Product datasheet		