1. General Description

The EXS0108 is a 8-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 8-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). $V_{CC(A)}$ can be supplied at any voltage between 1.3 V and 5.5 V and $V_{CC(B)}$ can be supplied at any voltage between 1.65 V and 5.5 V, making the device suitable for translating between any of the voltage nodes (1.8 V, 2.5 V, 3.3 V and 5.0 V). Pins An and OE are referenced to $V_{CC(A)}$ and pins Bn are referenced to $V_{CC(B)}$. A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and Benefits

■ Wide supply voltage range:

- $V_{CC(A)}$: 1.3 V to 5.5 V and $V_{CC(B)}$: 1.65 V to 5.5 V

■ Maximum data rates:

- Push-pull: 40 Mbps
- Open-drain: 2 Mbps

■ I_{OFF} circuitry provides partial Power-down mode operation

■ Inputs accept voltages up to 5.5 V

■ No power-supply sequencing required – V_{CCA} or V_{CCB} can be ramped first

■ Latch-up performance exceeds 100 mA per JESD 78B Class II

■ ESD protection:

- HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2500 V
- CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

■ Multiple package options

■ Specified from -40 °C to +85 °C and -40 °C to +125 °C

3.Ordering Information

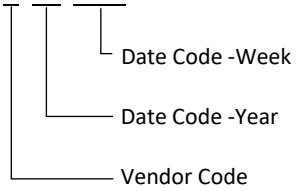
Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Quantity
EXS0108PW	S0108 XYYWW	TSSOP-20L	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	3000
EXS0108UD	S0108 XYYWW	QFN3x3-20L	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 3 × 3 × 0.8 mm	3000

MARKING INFORMATION

NOTE: XYYWW = Vendor Code and Date Code.

X YY WW



4.Function Diagram

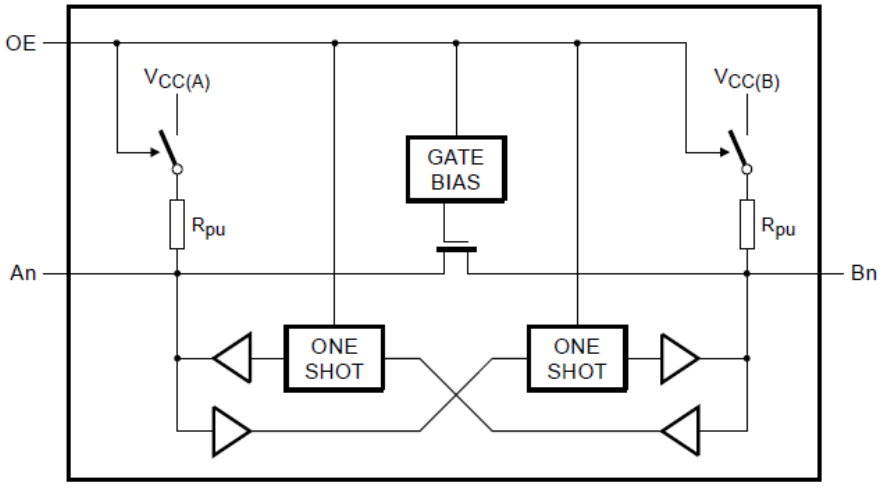


Fig. 1. Logic symbol （one channel）

5.Pinning Information

5.1. Pinning

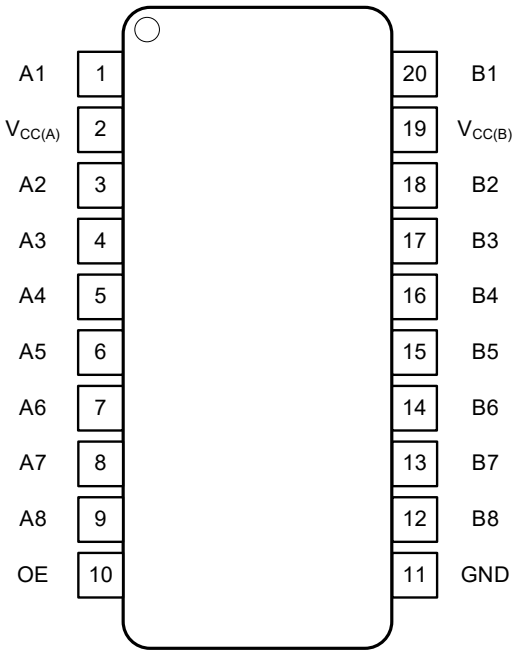


Fig. 2. Top view pin configuration TSSOP

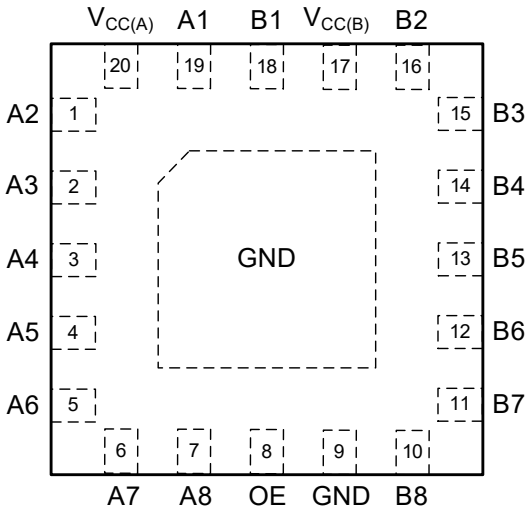


Fig. 3. Top view pin configuration QFN20L

5.2. Pin description

Table 2. Pin description

Symbol	Pin		Description
	TSSOP20L	QFN20L	
$V_{CC(A)}$	2	20	supply voltage A
A1,A2,A3,A4,A5,A6,A7,A8	1,3,4,5,6,7,8,9	19,1,2,3,4,5,6,7	data input or output (referenced to $V_{CC(A)}$)
GND	11	9	ground (0V)
OE	10	8	output enable input (active HIGH; referenced to $V_{CC(A)}$)
B8,B7,B6,B5,B4,B3,B2,B1	12,13,14,15,16,17,18,20	10,11,12,13,14,15,16,18	data input or output (referenced to $V_{CC(B)}$)
$V_{CC(B)}$	19	17	supply voltage B

6. Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state

Supply voltage		Input	Input/output	
$V_{CC(A)}$ [1]	$V_{CC(B)}$	OE	An	Bn
1.3 V to 5.5 V	1.65 V to 5.5 V	L	Z	Z
1.3 V to 5.5 V	1.65 V to 5.5 V	H	input or output	output or input
GND [2]	GND [2]	X	Z	Z

[1] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.

[2] When either $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into power-down mode.

7. Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 4. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	6.5	V
$V_{CC(B)}$	supply voltage B		-0.5	6.5	V
V_I	input voltage	OE [1]	-0.5	6.5	V
		An, Bn; Power-down or 3-state mode [1]	-0.5	6.5	V
		An, Bn; Active mode [1] [2] [3]	-0.5	V_{CCI}+0.5	V
V_O	output voltage	An, Bn; Power-down or 3-state mode [1]	-0.5	6.5	V
		An, Bn; Active mode [1] [3] [4]	-0.5	V_{CCO}+0.5	V
I_{IK}	input clamping current	V_I < 0 V	-50		mA
I_{OK}	output clamping current	V_O < 0 V	-50		mA
I_O	output current	V_O = 0 V to V_{CCO} [2]		±50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$		100	mA
I_{GND}	ground current		-100		mA
P_{tot}	total power dissipation	T_{amb} = -40 °C to + 125 °C		250	mW
T_{stg}	storage temperature		-65	150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] V_{CCI} is the supply voltage associated with the input.
[3] V_{CCI} + 0.5 V or V_{CCO} + 0.5 V should not exceed 6.5 V.
[4] V_{CCO} is the supply voltage associated with the output.

8. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 5. Recommended Operating Conditions[1] [2]

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		1.3	5.5	V
$V_{CC(B)}$	supply voltage B		1.65	5.5	V
V_I	input voltage	OE	0	5.5	V
		Power-down or 3-state mode			
		An	0	5.5	V
		Bn	0	5.5	V
		Active mode			
		An, Bn [3]	0	V_{CCI}	V
V_O	output voltage	Power-down or 3-state mode			
		An	0	5.5	V
		Bn	0	5.5	V
		Active mode			
		An, Bn [4]	0	V_{CCO}	V
T_{amb}	ambient temperature		-40	125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	A or B port; push-pull driving			
		$V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		10	ns/V
		OE input			
		$V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		10	ns/V

[1] The A and B sides of an unused I/O pair must be held in the same state, both at V_{CCI} or both at GND.
[2] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.
[3] V_{CCI} is the supply voltage associated with the input.
[4] V_{CCO} is the supply voltage associated with the output.

9. Static Characteristics

Table 6. Typical supply current

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

$V_{CC(A)}$	$V_{CC(B)}$								Unit
	1.8 V		2.5 V		3.3 V		5.0 V		
	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	
1.3 V	0.06	0.002	0.16	0.02	0.30	0.14	0.52	0.70	µA
1.5 V	0.06	0.002	0.16	0.008	0.32	0.10	0.60	0.60	µA
1.8 V	0.06	0.002	0.16	0.002	0.32	0.06	0.66	0.50	µA
2.5 V			0.14	0.002	0.32	0.002	0.80	0.26	µA
3.3 V					0.32	0.002	0.84	0.10	µA
5.0 V							0.86	0.02	µA

Table 7. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V). All typical values are measured at T_{amb} = 25°C. [1]

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
V_{IH}	HIGH-level input voltage	A port						
		$V_{CC(A)}$ = 1.3 V to 1.95 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	$V_{CC(A)}$ - 0.2		$V_{CC(A)}$	$V_{CC(A)}$ - 0.2	$V_{CC(A)}$	V
		$V_{CC(A)}$ = 2.3 V to 5.5 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	$V_{CC(A)}$ - 0.4		$V_{CC(A)}$	$V_{CC(A)}$ - 0.4	$V_{CC(A)}$	V
		B port						
		$V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	$V_{CC(B)}$ - 0.4		$V_{CC(B)}$	$V_{CC(B)}$ - 0.4	$V_{CC(B)}$	V
		OE input						
		$V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	$0.65V_{CC(A)}$		$V_{CC(A)}$	$0.65V_{CC(A)}$	$V_{CC(A)}$	V
V_{IL}	LOW-level input voltage	A or B port						
		$V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	0		0.15	0	0.15	V
		OE input						
		$V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	0		$0.35V_{CC(A)}$	0	$0.35V_{CC(A)}$	V
V_{OH}	HIGH-level output voltage	A port; I_O = -20 µA; $V_I \geq V_{CC(B)}$ - 0.4 V						
		$V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	$0.67V_{CC(A)}$			$0.67V_{CC(A)}$		V
		B port; I_O = -20 µA; $V_I \geq V_{CC(A)}$ - 0.2 V						
		$V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	$0.67V_{CC(B)}$			$0.67V_{CC(B)}$		V

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
V_{OL}	LOW-level output voltage	A or B port; IO = 1 mA; VI ≤ 0.15 V						
		$V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V			0.4		0.4	V
I_{OZ}	OFF-state output current	A or B port; $V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65V to 5.5 V			±4		±20	µA
I_I	input leakage current	OE input; $V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65V to 5.5 V			±4		±20	µA
I_{OFF}	power-off leakage current	A port; V_I or V_O = 0 V to 5.5 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0 V to 5.5 V			±4		±20	µA
		B port; V_I or V_O = 0 V to 5.5 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0 V to 5.5 V			±4		±20	µA
I_{CC}	supply current	OE = 0 V or $V_{CC(A)}$; An, Bn open						
		$I_{CC(A)}$						
		$V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V			12		54	µA
		$V_{CC(A)}$ = 5.5 V; $V_{CC(B)}$ = 0 V			3.7		19	µA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V			-1		-1	µA
		$I_{CC(B)}$						
		$V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V			11		53	µA
		$V_{CC(A)}$ = 5.5 V; $V_{CC(B)}$ = 0 V			-1		-1	µA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V			3.7		19	µA
		$I_{CC(A)}$ + $I_{CC(B)}$						
		$V_{CC(A)}$ = 1.3 V to 5.5 V; $V_{CC(B)}$ = 1.65 V to 5.5 V			21		105	µA
C_I	input capacitance	OE input; $V_{CC(A)}$ = 3.3 V; $V_{CC(B)}$ = 3.3 V		4				pF
$C_{I/O}$	input/output capacitance	A port; $V_{CC(A)}$ = 3.3 V; $V_{CC(B)}$ = 3.3 V						
		enabled		7				pF
		disabled		3.1				pF

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
		B port; $V_{CC(A)}$ = 3.3 V; $V_{CC(B)}$ = 3.3 V						
		enabled		7				pF
		disabled		3.1				pF

[1] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.

10. Dynamic Characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions	$V_{CC(B)}$				Unit
			1.8±0.15 V	2.5 V ± 0.2 V	3.3 V ± 0.3 V	5.0 V ± 0.5 V	
			Typ	Typ	Typ	Typ	
$V_{CC(A)}$ = 1.3 V; T_{amb} = 25℃							
t_{PHL}	HIGH to LOW propagation delay	A to B	4.9	6.5	7.8	9.5	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	8.6	6.9	6.2	6.0	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	4.5	5.6	6.5	8.7	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	5.8	5.1	4.9	4.8	ns
t_{en}	enable time	OE to A, B ; see Fig.5 [1]	82	82	82	82	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]	190	190	190	190	ns
		OE to B see Fig.6 [1]	174	137	182	131	ns
t_{TLH}	LOW to HIGH output transition time	A port	7.4	6.7	6.7	6.5	ns
		B port	10.2	8.2	6.6	6.5	ns
t_{THL}	HIGH to LOW output transition time	A port	7.3	7.3	7.6	7.6	ns
		B port	9.3	12.8	11.2	17.1	ns
$t_{sk(O)}$	output skew time	between channels [2]	0.7	0.7	0.7	0.7	ns

t_W	pulse width	data inputs	25	25	25	25	ns
f_{data}	data rate		40	40	40	40	Mbps

Table 9. Dynamic characteristics for temperature range -40 °C to +85 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8±0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.5 V ± 0.1V											
t_{PHL}	HIGH to LOW propagation delay	A to B		6.0		7.0		8.6		10.5	ns
t_{PLH}	LOW to HIGH propagation delay	A to B		12.6		10.0		8.5		8.0	ns
t_{PHL}	HIGH to LOW propagation delay	B to A		5.1		5.5		5.9		6.5	ns
t_{PLH}	LOW to HIGH propagation delay	B to A		8.5		8.0		5.8		5.5	ns
t_{en}	enable time	OE to A, B ; see Fig.5 [1]		120		120		120		120	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]		230		230		230		230	ns
		OE to B see Fig.6 [1]		200		150		180		115	ns
t_{TLH}	LOW to HIGH output transition time	A port	2.5	10.6	2.1	9.5	1.9	9.1	1.9	8.9	ns
		B port	4.1	15.2	3.2	10.6	2.8	8.7	0.4	7.5	ns
t_{THL}	HIGH to LOW output transition time	A port	3.0	9.7	3.1	10.8	3.1	10.1	3.1	10.2	ns
		B port	3.0	11.7	3.6	15.7	4.2	14.2	5.5	21.4	ns
$t_{sk(O)}$	output skew time	between channels [2]				0.7		0.7		0.7	ns
t_W	pulse width	data inputs			25		25		25		ns
f_{data}	data rate					40		40		40	Mbps
$V_{CC(A)}$ = 1.8 V ± 0.15 V											
t_{PHL}	HIGH to LOW propagation delay	A to B		4.5		5.0		5.5		7.5	ns
t_{PLH}	LOW to HIGH propagation delay	A to B		11.3		8.4		6.4		6.1	ns

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8±0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PHL}	HIGH to LOW propagation delay	B to A		3.5		4.1		4.5		5.5	ns
t_{PLH}	LOW to HIGH propagation delay	B to A		6.5		6.0		5.0		4.6	ns
t_{en}	enable time	OE to A, B ; see Fig.5 [1]		100		100		100		100	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]		200		200		200		200	ns
		OE to B see Fig.6 [1]		200		150		180		115	ns
t_{TLH}	LOW to HIGH output transition time	A port	2.3	8.7	1.8	7.6	1.6	7.4	1.5	7.1	ns
		B port	3.9	14.2	3.1	9.8	2.7	7.7	2.3	6.8	ns
t_{THL}	HIGH to LOW output transition time	A port	2.7	9.2	2.7	9.3	2.7	9.7	2.9	9.8	ns
		B port	2.6	9.6	2.9	12.0	3.3	9.8	4.3	15.0	ns
$t_{sk(O)}$	output skew time	between channels [2]				0.7		0.7		0.7	ns
t_W	pulse width	data inputs			25		25		25		ns
f_{data}	data rate					40		40		40	Mbps
$V_{CC(A)}$ = 2.5 V ± 0.2 V											
t_{PHL}	HIGH to LOW propagation delay	A to B				2.5		2.7		3.8	ns
t_{PLH}	LOW to HIGH propagation delay	A to B				5.7		5.0		5.2	ns
t_{PHL}	HIGH to LOW propagation delay	B to A				2.8		3.5		4.2	ns
t_{PLH}	LOW to HIGH propagation delay	B to A				1.8		1.6		1.5	ns
t_{en}	enable time	OE to A, B ; see Fig.5 [1]				80		80		80	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]				150		150		150	ns
		OE to B see Fig.6 [1]				150		180		115	ns

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8±0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{TLH}	LOW to HIGH output transition time	A port			1.7	6.3	1.4	5.9	1.3	5.7	ns
		B port			2.7	9.1	2.4	7.1	2.1	6.0-	ns
t_{THL}	HIGH to LOW output transition time	A port			2.4	9.9	2.5	10.1	2.5	10.3	ns
		B port			2.3	9.8	2.5	7.4	3.0	10.5	ns
$t_{sk(O)}$	output skew time	between channels [2]				0.7		0.7		0.7	ns
t_W	pulse width	data inputs			25		25		25		ns
f_{data}	data rate					40		40		40	Mbps
$V_{CC(A)}$ = 3.3 V ± 0.3 V											
t_{PHL}	HIGH to LOW propagation delay	A to B						1.9		2.7	ns
t_{PLH}	LOW to HIGH propagation delay	A to B						3.0		3.5	ns
t_{PHL}	HIGH to LOW propagation delay	B to A						3.0		3.5	ns
t_{PLH}	LOW to HIGH propagation delay	B to A						1.9		1.7	ns
t_{en}	enable time	OE to A, B ; see Fig.5 [1]						70		70	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]						180		180	ns
		OE to B see Fig.6 [1]						180		115	ns
t_{TLH}	LOW to HIGH output transition time	A port					1.4	4.7	1.2	4.3	ns
		B port					2.2	6.6	2	5.8	ns
t_{THL}	HIGH to LOW output transition time	A port					2.3	7.3	2.3	7.9	ns
		B port					2.3	6.9	2.5	9.6	ns
$t_{sk(O)}$	output skew time	between channels [2]						0.7		0.7	ns
t_W	pulse width	data inputs	25		25		25		25		ns
f_{data}	data rate			40		40		40		40	Mbps

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8±0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 5.5 V ± 0.5 V											
t_{PHL}	HIGH to LOW propagation delay	A to B								1.8	ns
t_{PLH}	LOW to HIGH propagation delay	A to B								1.5	ns
t_{PHL}	HIGH to LOW propagation delay	B to A								2.5	ns
t_{PLH}	LOW to HIGH propagation delay	B to A								2.3	ns
t_{en}	enable time	OE to A, B ; see Fig.5 [1]								60	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]								115	ns
		OE to B see Fig.6 [1]								115	ns
t_{TLH}	LOW to HIGH output transition time	A port							1.4	6.0	ns
		B port							1.8	5.8	ns
t_{THL}	HIGH to LOW output transition time	A port							2.2	9.4	ns
		B port							2.2	9.2	ns
$t_{sk(O)}$	output skew time	between channels [2]						0.7		0.7	ns
t_W	pulse width	data inputs	25		25		25		25		ns
f_{data}	data rate			40		40		40		40	Mbps

[1] t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[2] Skew between any two outputs of the same package switching in the same direction.

Table 10. Dynamic characteristics for temperature range -40 °C to +125 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8±0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.5 V ± 0.1V											
t_{PHL}	HIGH to LOW propagation delay	A to B		6.0		7.0		8.6		10.5	ns
t_{PLH}	LOW to HIGH propagation delay	A to B		12.6		10.5		9.2		8.5	ns
t_{PHL}	HIGH to LOW propagation delay	B to A		5.1		5.5		5.9		6.5	ns
t_{PLH}	LOW to HIGH propagation delay	B to A		8.5		8.0		5.8		5.5	ns
t_{en}	enable time	OE to A, B ; see Fig.5 [1]		120		120		120		120	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]		230		230		230		230	ns
		OE to B see Fig.6 [1]		200		150		180		115	ns
t_{TLH}	LOW to HIGH output transition time	A port	2.5	10.8	2.1	9.6	1.9	9.3	1.9	9.9	ns
		B port	4.1	15.3	3.2	10.9	2.8	8.9	0.4	7.7	ns
t_{THL}	HIGH to LOW output transition time	A port	3.0	9.7	3.1	10.8	3.1	10.1	3.1	10.2	ns
		B port	3.0	11.7	3.6	15.7	4.2	14.2	5.5	21.4	ns
$t_{sk(O)}$	output skew time	between channels [2]				0.8		0.8		0.8	ns
t_W	pulse width	data inputs			25		25		25		ns
f_{data}	data rate					40		40		40	Mbps
$V_{CC(A)}$ = 1.8 V ± 0.15 V											
t_{PHL}	HIGH to LOW propagation delay	A to B		4.5		5.0		5.5		7.5	ns
t_{PLH}	LOW to HIGH propagation delay	A to B		11.3		9.0		7.1		6.7	ns
t_{PHL}	HIGH to LOW propagation delay	B to A		3.5		4.1		4.5		5.5	ns

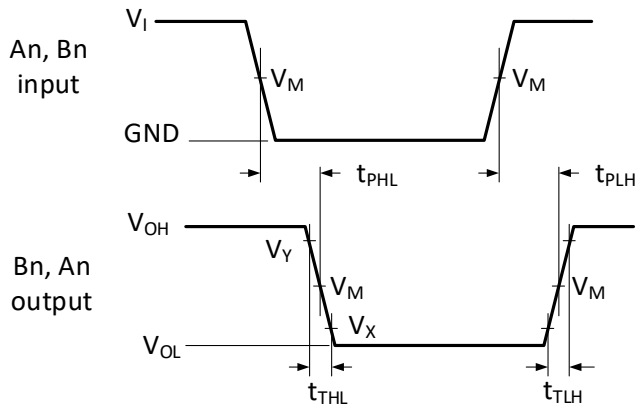
Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8±0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}	LOW to HIGH propagation delay	B to A		6.5		6.0		5.0		4.6	ns
t_{en}	enable time	OE to A, B ; see Fig.5 [1]		100		100		100		100	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]		200		200		200		200	ns
		OE to B see Fig.6 [1]		200		150		180		115	ns
t_{TLH}	LOW to HIGH output transition time	A port	2.3	8.9	1.8	7.8	1.6	7.6	1.5	7.3	ns
		B port	3.9	14.3	3.1	10.1	2.7	7.9	2.3	7.4	ns
t_{THL}	HIGH to LOW output transition time	A port	2.7	9.2	2.7	9.3	2.7	9.7	2.9	9.8	ns
		B port	2.6	9.6	2.9	12.0	3.3	9.8	4.3	15.0	ns
$t_{sk(O)}$	output skew time	between channels [2]				0.8		0.8		0.8	ns
t_W	pulse width	data inputs			25		25		25		ns
f_{data}	data rate					40		40		40	Mbps
$V_{CC(A)}$ = 2.5 V ± 0.2 V											
t_{PHL}	HIGH to LOW propagation delay	A to B				2.7		2.9		4.1	ns
t_{PLH}	LOW to HIGH propagation delay	A to B				5.7		5.5		5.8	ns
t_{PHL}	HIGH to LOW propagation delay	B to A				2.8		4.0		5.3	ns
t_{PLH}	LOW to HIGH propagation delay	B to A				1.8		1.6		1.7	ns
t_{en}	enable time	OE to A, B ; see Fig.5 [1]				80		80		80	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]				150		150		150	ns
		OE to B see Fig.6 [1]				150		180		115	ns
t_{TLH}	LOW to HIGH output transition time	A port			1.7	6.5	1.4	6.1	1.3	5.8	ns
		B port			2.7	9.3	2.4	7.3	2.1	6.2	ns

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8±0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{THL}	HIGH to LOW output transition time	A port			2.4	9.9	2.5	10.1	2.5	10.3	ns
		B port			2.3	9.8	2.5	7.4	3.0	10.5	ns
$t_{sk(O)}$	output skew time	between channels [2]				0.8		0.8		0.8	ns
t_W	pulse width	data inputs			25		25		25		ns
f_{data}	data rate					40		40		40	Mbps
$V_{CC(A)}$ = 3.3 V ± 0.3 V											
t_{PHL}	HIGH to LOW propagation delay	A to B						2.1		3.0	ns
t_{PLH}	LOW to HIGH propagation delay	A to B						3.0		4.0	ns
t_{PHL}	HIGH to LOW propagation delay	B to A						3.5		4.0	ns
t_{PLH}	LOW to HIGH propagation delay	B to A						1.9		1.7	ns
t_{en}	enable time	OE to A, B ; see Fig.5 [1]						70		70	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]						180		180	ns
		OE to B see Fig.6 [1]						180		115	ns
t_{TLH}	LOW to HIGH output transition time	A port					1.4	4.8	1.2	4.4	ns
		B port					2.2	6.9	2	6.1	ns
t_{THL}	HIGH to LOW output transition time	A port					2.3	7.3	2.3	7.9	ns
		B port					2.3	6.9	2.5	9.6	ns
$t_{sk(O)}$	output skew time	between channels [2]						0.8		0.8	ns
t_W	pulse width	data inputs	25		25		25		25		ns
f_{data}	data rate			40		40		40		40	Mbps
$V_{CC(A)}$ = 5.5 V ± 0.5 V											
t_{PHL}	HIGH to LOW propagation delay	A to B								1.9	ns

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8±0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}	LOW to HIGH propagation delay	A to B								1.8	ns
t_{PHL}	HIGH to LOW propagation delay	B to A								3.0	ns
t_{PLH}	LOW to HIGH propagation delay	B to A								2.3	ns
t_{en}	enable time	OE to A, B ; see Fig.5 [1]								60	ns
t_{dis}	disable time	OE to A; see Fig.6 [1]								115	ns
		OE to B see Fig.6 [1]								115	ns
t_{TLH}	LOW to HIGH output transition time	A port							1.4	6.5	ns
		B port							1.8	6.2	ns
t_{THL}	HIGH to LOW output transition time	A port							2.2	9.5	ns
		B port							2.2	9.3	ns
$t_{sk(O)}$	output skew time	between channels [2]								0.8	ns
t_W	pulse width	data inputs	25		25		25		25		ns
f_{data}	data rate			40		40		40		40	Mbps

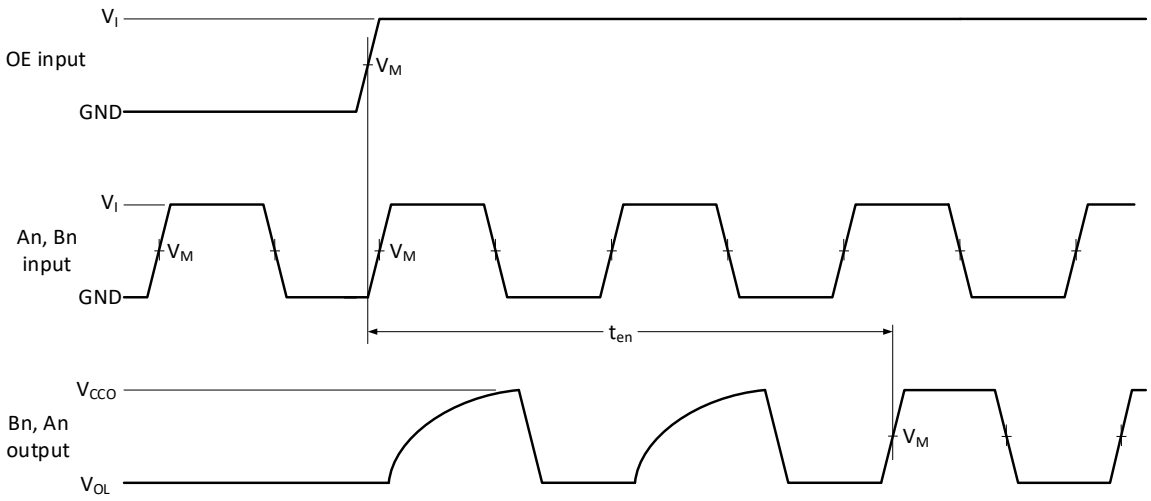
[1] t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[2] Skew between any two outputs of the same package switching in the same direction.

10.1. Waveforms and test circuit



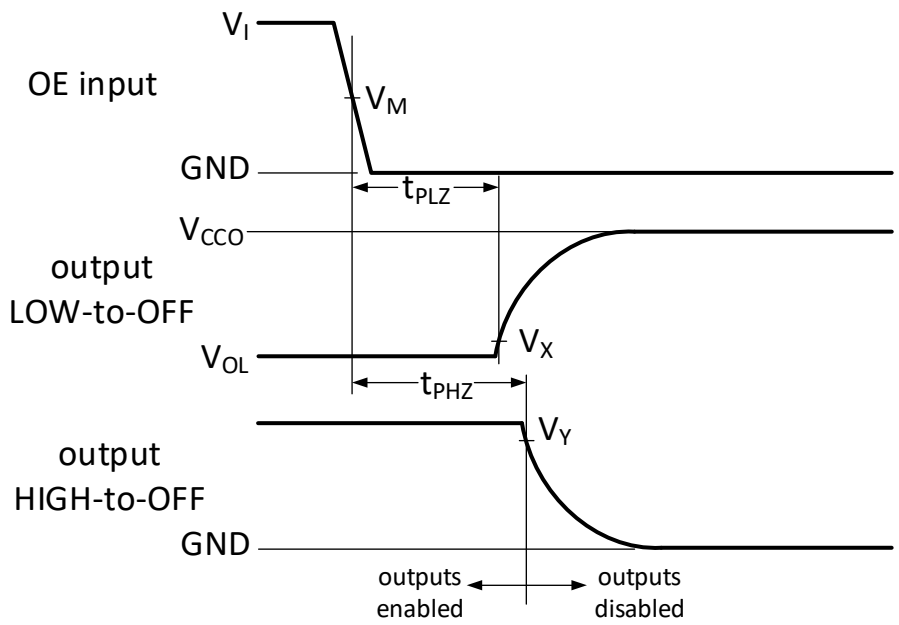
Measurement points are given in Table 11.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 4. The data input (An, Bn) to data output (Bn, An) propagation delay times



(1) The enable time (ten) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. See also Section 11.6
Measurement points are given in Table 11.
V_{OL} is a typical output voltage level that occur with the output load.
V_{CCO} is the supply voltage associated with the output.

Fig. 5. Enable times



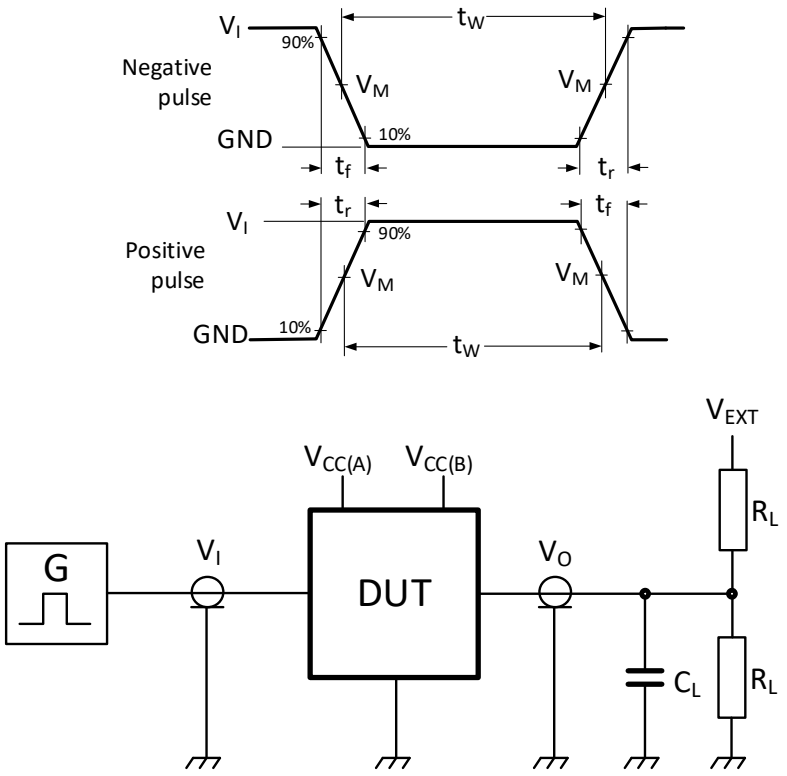
Measurement points are given in Table 11.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.
V_{CCO} is the supply voltage associated with the output.

Fig. 6. Disable times

Table 11. Measurement points

Supply Voltage	Input	Output		
V_{CCO}	V_M	V_M	V_X	V_Y
1.5 V ± 0.1 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
1.8 V ± 0.15 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.5 V ± 0.2 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
3.3 V ± 0.3 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V
5.0 V ± 0.5 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V

[1] V_{CCI} is the supply voltage associated with the input.
[2] V_{CCO} is the supply voltage associated with the output.



Test data is given in Table 12.
All input pulses are supplied by generators having the following characteristics:
PRR ⩽ 10 MHz; Z_O = 50 Ω; dt/dV ⩽ 2.5 ns/V.
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
V_{EXT} = External voltage for measuring switching times.

Fig. 7. Test circuit for measuring switching times

Table 12. Test data

Supply voltage		Input		Load		V_{EXT}		
$V_{CC(A)}$	$V_{CC(B)}$	V_I [1]	Δt/ΔV	C_L	R_L [2]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.3 V to 5.5 V	1.65 V to 5.5 V	V_{CCI}	≤2.5 ns/V	15 pF	50 kΩ, 1MΩ	open	open	$2V_{CCO}$

[1] V_{CCI} is the supply voltage associated with the input.
[2] For measuring data rate, pulse width, propagation delay and output rise and fall measurements, R_L = 1 MΩ. For measuring enable and disable times, R_L = 50 kΩ.
[3] V_{CCO} is the supply voltage associated with the output.

11. Application information

11.1. Applications

Voltage level-translation applications. The EXS0108 can be used in point-to-point applications to interface between devices or systems operating at different supply voltages. The device is primarily targeted at I^2C or 1-wire which use open-drain drivers, it may also be used in applications where push-pull drivers are connected to the ports.

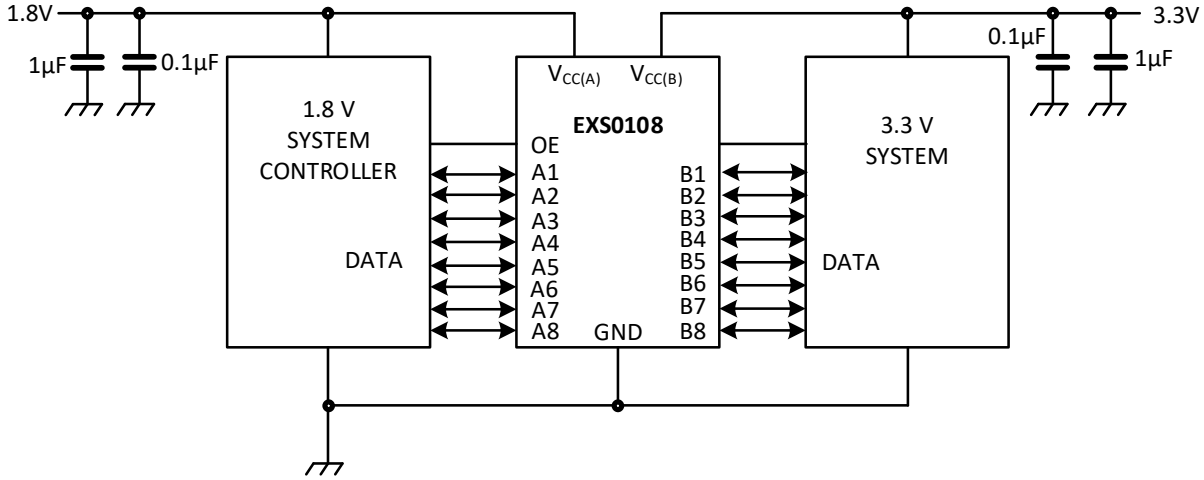


Fig. 8. Typical operating circuit

11.2. Architecture

The architecture of the EXS0108 is shown in Fig. 1. The device does not require an extra input signal to control the direction of data flow from A to B or B to A.

The EXS0108 is a "switch" type voltage translator, it employs two key circuits to enable voltage translation:

1. A pass-gate transistor (N-channel) that ties the ports together.
2. An output edge-rate accelerator that detects and accelerates rising edges on the I/O pins.

The gate bias voltage of the pass gate transistor (T3) is set at approximately one threshold voltage above the V_{CC} level of the low-voltage side. During a LOW-to-HIGH transition the output one-shot accelerates the output transition by switching on the PMOS transistors (T1, T2) bypassing the 10 kΩ pull-up resistors and increasing current drive capability. The one-shot is activated once the input transition reaches approximately $0.5V_{CCI}$. During the acceleration time the driver output resistance is between approximately 50 Ω and 70 Ω.

To avoid signal contention and minimize dynamic I_{CC}, the user should wait for the one-shot circuit to turn-off before applying a signal in the opposite direction. Pull-up resistors are included in the device for DC current sourcing capability.

11.3. Input driver requirements

As the EXS0108 is a switch type translator, properties of the input driver directly effect the output signal. The external open-drain or push-pull driver applied to an I/O determines the static current sinking capability of the system; the max data rate, HIGH-to-LOW output transition time (t_{THL}) and propagation delay (t_{PHL}) are dependent upon the output impedance and edge-rate of the external driver. The limits provided for these parameters in the datasheet assume a driver with output impedance below 50 Ω is used.

11.4. Output load considerations

The maximum lumped capacitive load that can be driven is dependant upon the one-shot pulse duration. In cases with very heavy capacitive loading there is a risk that the output will not reach the positive rail within the one-shot pulse duration.To avoid excessive capacitive loading and to ensure correct triggering of the one-shot it's recommended to use short trace lengths and low capacitance connectors on EXS0108 PCB layouts. To ensure low impedance termination and avoid output signal oscillations and one-shot re-triggering, the length of the PCB trace should be such that the round trip delay of any reflection is within the one-shot pulse duration.

11.5. Power up

During operation $V_{CC(A)}$ must never be higher than $V_{CC(B)}$, however during power-up $V_{CC(A)} \geqslant V_{CC(B)}$ does not damage the device, so any power supply can be ramped up first. There is no special power-up sequencing required. The EXS0108 includes circuitry that disables all output ports when either $V_{CC(A)}$ or $V_{CC(B)}$ is switched off.

11.6. Enable and disable

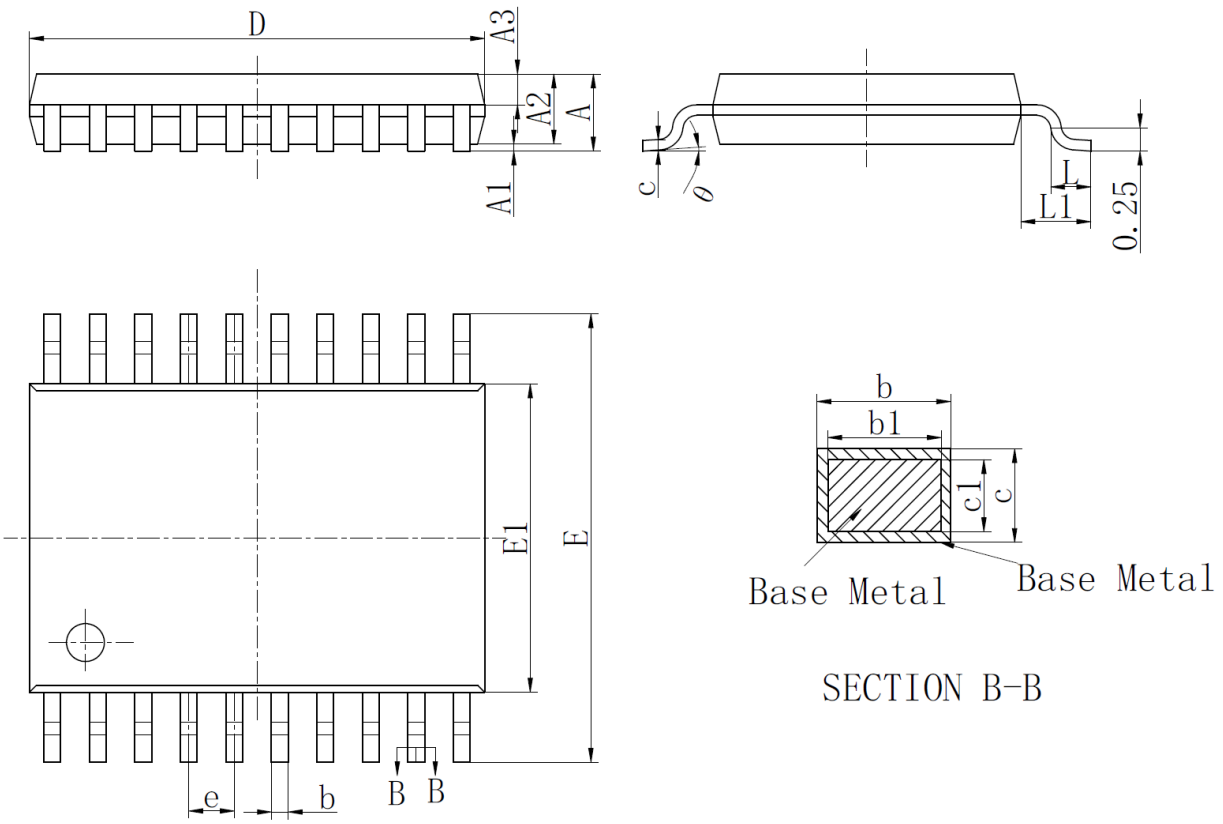
An output enable input (OE) is used to disable the device. Setting OE to LOW causes all I/Os to assume the high-impedance OFF-state. The disable time (t_{dis} with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time (t_{en}) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor, the minimum value of the resistor is determined by the current-sourcing capability of the driver.

11.7. Pull-up or pull-down resistors on I/O lines

Each A port I/O has an internal 10 kΩ pull-up resistor to $V_{CC(A)}$, and each B port I/O has an internal 10 kΩ pull-up resistor to $V_{CC(B)}$. If a smaller value of pull-up resistor is required, an external resistor must be added parallel to the internal 10 kΩ, this will effect the V_{OL} level. When OE goes LOW the internal pull-ups of the EXS0108 are disabled.

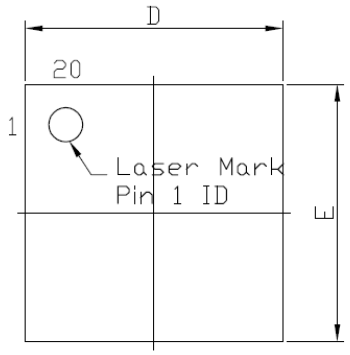
12. Package Outline

TSSOP-20L

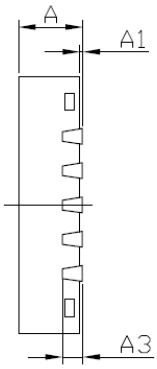


Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min.	Max.		Min.	Max.
A	-	1.20	E	6.20	6.60
A1	0.05	0.15	e	0.65BSC	
A2	0.80	1.05	L	0.45	0.75
A3	0.39	0.49	L1	1.00REF	
b	0.20	0.28	θ	0°	8°
b1	0.19	0.25			
c	0.13	0.17			
c1	0.12	0.14			
D	6.40	6.60			
E1	4.30	4.50			

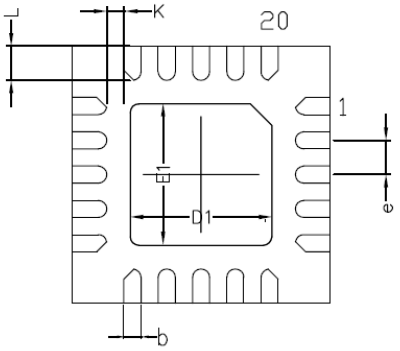
QFN3x3-20L



Top View



Side View



bottom View

Symbol	Dimensions In Millimeters			Symbol	Dimensions In Millimeters		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	0.70	0.75	0.80	D1	1.55	1.65	1.75
A1	0.00	-	0.05	E1	1.55	1.65	1.75
A3	0.203REF			e	0.40TYP		
b	0.15	-	0.25	K	0.20	-	-
D	2.90	3.00	3.10	L	0.30	0.40	0.50
E	2.90	3.00	3.10				

13. Tape and Reel Information

13.1. Carrier tape dimensions

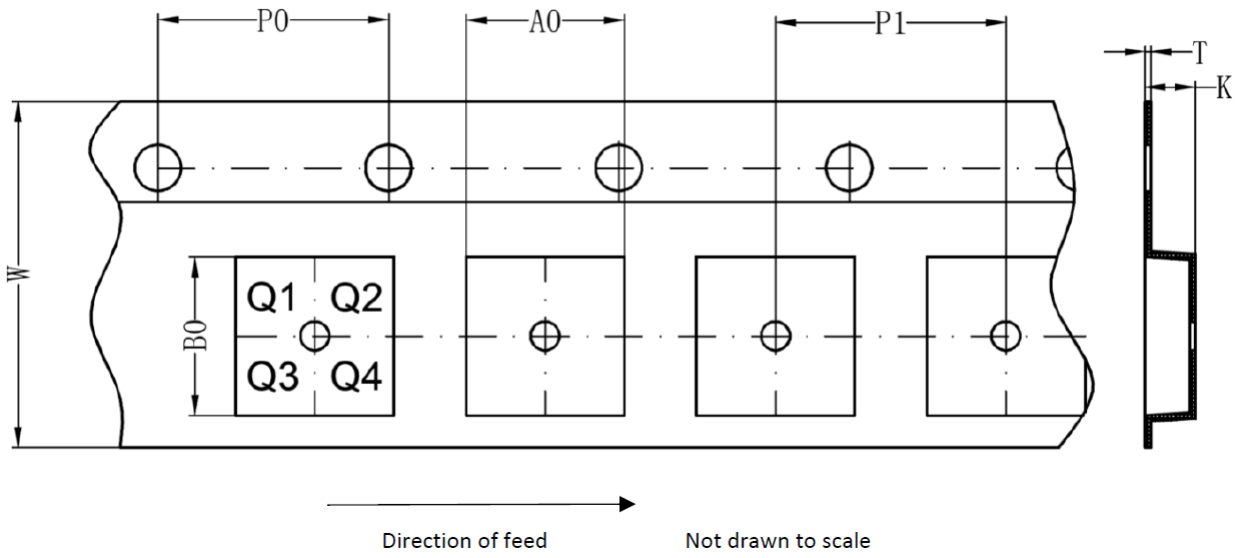


Table 13. Carrier tape dimensions

Package version	A0(mm)	B0(mm)	K(mm)	T(mm)	P1(mm)	W(mm)	P0(mm)	PIN 1
TSSOP-20L	6.85	6.85	1.7	0.22	8	12	4	Q1

13.2. Reel and box dimensions

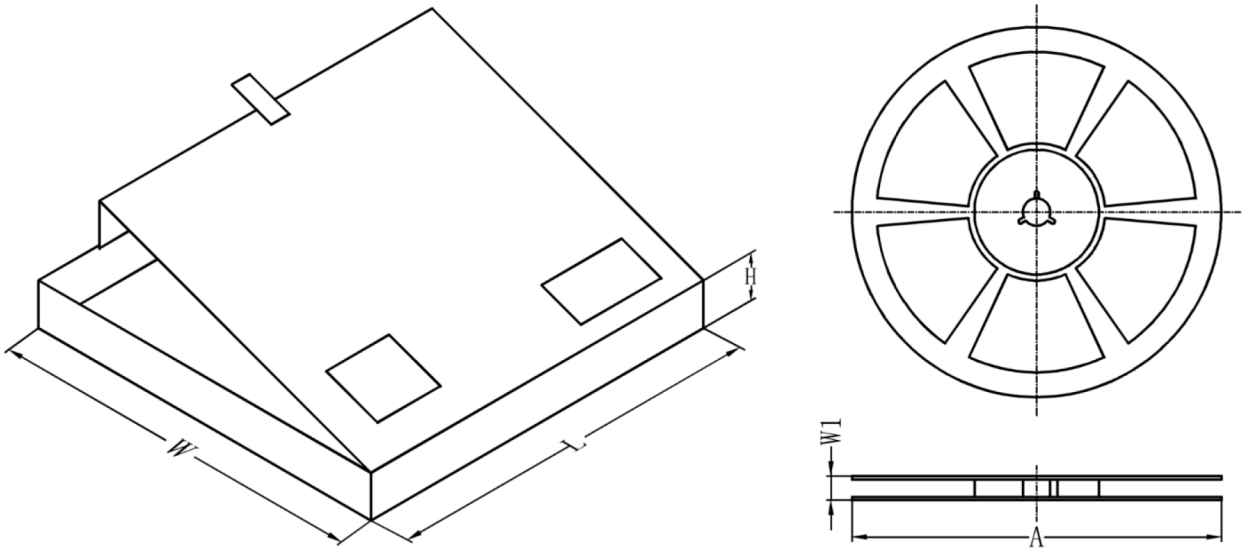


Table 14. Dimensions and quantities

Package version	Type NO.ending	Reel Dimension A(mm)	ReelWidth W1(mm)	SPQ (pcs)	Reels per box	Outer box dimensions L×W×H(mm)
TSSOP-20L	PW	330	18.4	3000	1	358x340x50

14. Abbreviations

Table 15. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model
I^2C	Inter-Integrated Circuit
PCB	Printed Circuit Board
PRR	Pulse Rate Repetition

15. Revision History

Table 16. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
EXS0108 Rev. 1.0	Oct 25, 2025	Product datasheet		